Performance of Low Power SRAM Cells On SNM and Power Dissipation

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Abstract: Over the years, power requirement reduction in SRAM has undergone tremendous advancement. Many circuit techniques have been devised to achieve active and standby power reduction in both dynamic and static power. The ever increasing demand for larger data storage capacity has driven the fabrication technology and memory development towards more compact design rules and consequently, towards higher data storage densities. Thus, the maximum realizable data storage capacity of single chip semiconductor, memory circuits is approximately getting doubled every two years [3]. Cache memory plays a key role in high speed electronic gadgets. SRAM is the key element of cache memory. Cache memory is used for their high speed and SRAM is the element which provides speed to the cache. So this work is mainly concentrated on the ultra low power design and analysis SRAM cells. In the last three decades of semiconductor memories growth, the DRAMs have been the largest volume volatile memory produced for use as main computer memories because of their high density and low cost per bit advantage. SRAM densities have generally lagged a generation behind the DRAM. However, the SRAMs offer a low-power consumption and high-performance feature, which makes them practical alternatives to the DRAMs. Nowadays, a vast majority of SRAMs are being fabricated in the CMOS technologies for commodity SRAMs.

In this paper, we are proposing the low power reduction technique for SRAM Cell and calculating the SNM and power dissipation for Read, Write & Hold operation on 180nm technology using Mentor Graphics, IC Design tool. In this work, high performance and ultra low power issue of SRAM cells has been considered. So, it is necessary to shrink the area of SRAM cells. As technology shrinks, power consumption (mainly leakage in nano-regime) becomes an essential parameter.

KEYWORDS: SRAM, Low Power, SNM, READ, WRITE

1. INTRODUCTION

A major portion of silicon area of many digital designs is dedicated to memory. SRAM plays a key role in modern electronics high speed memory as the technology scales down and the need for high performance in very deep sub-micron CMOS design is on the increase. The data retention of the SRAM cell in hold state and the read state are important constraints in advanced CMOS technology nodes. The SRAM cell becomes less stable at low supply voltage (VDD), with increasing leakage currents and variability. CMOS scaling requires not only very low threshold voltages to retain the device switching speeds, but also ultra-thin gate oxides to maintain the current drive and keep threshold voltage variations under control when dealing with short-channel effects [1]. Low threshold voltage results in an increase in the sub threshold leakage current, whereas ultra-thin oxide causes an increase in the gate leakage current. Consequently, one way to reduce leakage current is to increase threshold voltage. CMOS technology scaling attempts to maintain a constant electric field while improving density, operation speed and consumption power. This law suggests that electric field in a device can be kept constant by scaling the device size and the operation voltage at the same pace. When the device geometry is shrunk by a factor of $k$, the delay is also reduced by the same factor. At the same time, supply voltage (VDD) should be reduced by a factor of $k$ in order to maintain a constant electric field. This, in turn, will result in a reduction in dynamic power consumption by a factor of square of $k$. The operation frequency for large-scale integrations (LSIs) has been increasing to satisfy the demand of high-speed systems. The increase in operation speed causes higher active power dissipation. Low supply voltage has been applied to decrease the power dissipation because active power is proportional to the square of VDD. Recently, technology has reached the region of VDD below 1 V and gate length below 40 nm [4].

The stability of SRAM is usually defined by the static noise margin (SNM) as the maximum value of the DC noise voltage that can be tolerated by the SRAM cell without altering the stored bits. As technology is shrinking, demand is increasing for better functionality, less silicon area, low power consumption, and longer battery life. So there is trade off between various performance parameters of SRAM cells. There are severe constraints for reliable write and read operation which affect the performance of SRAM cells. In the design of 6T SRAM cell, there can be variation in both the width and length of transistor, so aspect ratio can be varied. aspect ratio should be optimum for area centric design. Aspect ratio also affects the read and writes stability of SRAM cells. Higher threshold voltage transistors result in decreased sub-threshold leakage and increased of delay. For ultra low SRAM cells leakage current should be minimized. The performance parameters include trade off between small areas, large noise margin, lesser delay, low power operation, low
supply voltage [6]. This paper further divided as follows:
Section 2 describes working of SRAM Cells, Section 3 describes the Proposed CMOS Cells, Section 4 describe analysis and results & section 5 finally concludes the proposed work.

2. 6T CMOS SRAM CELL
As shown in Fig. 2.1 the conventional 6T memory cell comprises of two CMOS inverters cross coupled with two pass transistors connected to a complementary bit lines. In Fig.1.1 the access transistors NMOS_3 and NMOS_4 are connected to the wordline (WL) to have the data written to the memory cell from bit lines (BL). The bit lines act as I/O buses which carry the data from memory cells to the sense amplifier. The main operations of the SRAM cells are the write, read and hold. The SNM is an important performance factor of hold and read operations, specifically in read operation when the wordline is '1' and the bit lines are precharged to '1'. The internal node of SRAM which stores '0' will be pulled up through the access transistor across the access transistor and the drive transistor. This increase in voltage severely degrades the SNM during read operation. The read stability is mainly depended on the cell ratio.

![Figure 2.1. 6T CMOS SRAM cell.](image1)

Write Operation
For the write operation as shown in figure 2.2, in order to store a logic "1" to the cell, BL is charged to Vdd and BLB is charged to ground and vise versa for storing a logic '0'. Then the word line is switched to Vdd to turn ON the NMOS access transistor. When the access transistors are turned ON, the values of the bitlines are written into Node A and Node B. The node that is storing the logic "1" will not go to full Vdd because of a voltage drop across the NMOS access transistor. After the write operation the wordline voltage is reset to ground to turn off the NMOS access transistor. The node with the logic "1" stored will be pulled up to full Vdd through the PMOS driver transistors.

![Figure 2.2. 6T CMOS cell during write '0' operation.](image2)

Read Operation
For the read operation, the bitlines and wordlines are charged to Vdd. The node with logic "1" stored will pull the voltage on the corresponding bitlines up to a high (not Vdd because of the voltage drop across the NMOS access transistor) voltage level. The sense amplifier will detect the which bitline is at high voltage and which bitline is at ground. The circuit diagram is shown in figure 2.3.

![Figure 2.3. 6T CMOS cell during read '0' operation.](image3)

3. STATIC NOISE MARGI NOF SRAM
Noise margin can be defined using the input voltage to output voltage transfer characteristic (VTC). The static noise margin high and static noise margin low is defined as [14]

\[ NM_{H} = V_{OH} - V_{IH} \] (3.1)

\[ NM_{L} = V_{IL} - V_{OL} \] (3.2)

where \( V_{IL} \) is the maximum input voltage level recognized as logical "0", \( V_{IH} \) is the minimum input voltage level recognized as a logical "0", \( V_{OL} \) is the maximum logical "0" output voltage, \( V_{OH} \) is the minimum logical "1" output voltage.

3.1 Determination of SNM
SNM is determined as a side of the maximum square drawn between the inverter characteristics [19]. An important advantage of this method is that it can be automated using a DC circuit simulator, which to a great degree extends its practical usefulness. In this approach, an SRAM cell is presented as two equivalent inverters.
with the noise sources inserted between the corresponding inputs and outputs. Both series voltage noise sources (Vn) have the same value and act together to upset the state of the cell, i.e. they have an inverse polarity to the current state of each inverter of the cell. Applying the adverse noise sources polarity represents the worst-case equal noise margins. Figure 3.1 shows the superimposed normal inverter transfer curve of a read accessed 6T SRAM cell and its mirrored with respect to x = y line counterpart in a x − y coordinate system. This is a convenient arrangement. Since by knowing the diagonals of the maximum embedded squares we can calculate the sides.

![Figure 3.1 SNM estimation based on maximum square][14].

### 4. PROPOSED 6T SRAM CELL

In this proposed SRAM cell bulk bias technique as shown in the figure 4.1 are used in order to reduce the leakage power dissipation in active mode operation of SRAM cell. In our SRAM cell, the bulk (substrate) of inverters NMOS (which are connected back to back) is biased with some negative voltage and the bulk of NMOS access transistor is connected to the ground potential. In this work the optimum value of the bulk bias is calculated for both PMOS and NMOS transistor and that voltage is applied to the SRAM cells. By using the bulk bias technique threshold voltage of the transistors increases. So with increase in threshold voltage the problem of subthreshold leakage in CMOS transistor is solved and the leakage and average power dissipation of SRAM Cell is reduced.

![Figure 4.1. 6T Proposed SRAM cell][15]

### 5. ANALYSIS & RESULTS

The Simulation of SRAM Cell with and without low power techniques is carried out at 180nm CMOS technology parameters taken for NMOS and PMOS transistors, using TSPICE tool [11-12]. Transient analysis is done to get Power results and different operation of SRAM and DC analysis is done to get static noise margin.

#### 6T SRAM Cell Operations (without bulk bias)

In this section output waveforms are shown for different operations of 6T SRAM cell.

**Write Operation and Hold Operation:**

Fig 5.1 shown below shows the write and hold operation of 6T SRAM cell without any low power technique. The transient analysis is done for write and hold operation.

![Fig: 5.1 Write "1" (0-50ns) Hold "0" (50-100ns)]

**Write Operation and Read Operation:**

Fig 5.2 shown below shows the write and read operation of 6T SRAM cell without any low power technique. The transient analysis is done for write and read operation.

![Fig: 5.2 Write "0" (0-50ns) Read "0" (50-100ns)]

#### 5.1Comparison of 6T SRAM Cell Parameters (With and Without Bulk Bias Technique):

In this section comparison between 6T SRAM cell with and without bulk bias has been carried out on the basis of subthreshold leakage current, average power consumption in active mode operation of SRAM cell. Experimentally We have found that the optimum value for bulk bias of PMOS transistor is 1.8V and for NMOS transistor is -0.6V.

During Write "1" Operation:
Table 1 and figure 5.3 shown below shows the comparison of leakage currents and average power consumption, with and without bulk bias technique and also shows the percentage reduction by using optimum bulk bias during write “1” operation.

### Table 1

<table>
<thead>
<tr>
<th>During Write Operation</th>
<th>Without Bulk Bias</th>
<th>With Bulk Bias</th>
<th>% Reduction</th>
</tr>
</thead>
<tbody>
<tr>
<td>Id(MN莫斯_1)&lt;A&gt;</td>
<td>1.90E-11</td>
<td>4.33E-12</td>
<td>77%</td>
</tr>
<tr>
<td>Id(MNmos_3)&lt;A&gt;</td>
<td>1.8E-12</td>
<td>1.80E-12</td>
<td>No Effect</td>
</tr>
<tr>
<td>Id(MPmos_2)&lt;A&gt;</td>
<td>-6.33E-12</td>
<td>-6.33E-12</td>
<td>No Effect</td>
</tr>
<tr>
<td>Average power consumed -&gt;</td>
<td>4.88E-11</td>
<td>2.24E-11</td>
<td>54%</td>
</tr>
</tbody>
</table>

During write “1” operation transistors NMOS_1, NMOS_3 and PMOS_2 will be in cutoff region. The drain to source current flow from these transistors are leakage current.

**Fig: 5.3** Comparison Graph With and Without Bulk Bias Technique during write “1” Operation

From the Table 1 and graph shown in Fig 5.3 we can see that only subthreshold leakage current of NMOS_1 is reduced by 77% using bulk bias technique. The total power dissipation during write operation reduced up to 54% by using bulk bias technique.

### Average Power Consumed During Write and Hold Operation:

Table 2 and Fig:5.4 shows the comparison of average power consumed, with and without bulk bias technique and % reduction in average power consumption by using bulk bias technique during write (0-50ns) and hold(50-100ns) operation.

### Table 2

<table>
<thead>
<tr>
<th>During Write and Hold Operation</th>
<th>Without Bulk Bias</th>
<th>With Bulk Bias</th>
<th>% Reduction</th>
</tr>
</thead>
<tbody>
<tr>
<td>Average power consumed</td>
<td>2.77E-07</td>
<td>2.52E-07</td>
<td>9.31%</td>
</tr>
</tbody>
</table>

In Table:2, we can see that, when hold operation is done after write operation the total power dissipation is reduced up to 9.31% by using the optimum bulk bias technique.

### Average Power Consumed During Write and Read Operation:

Table 3 and Fig:5.5 shows the comparison of average power consumed, with and without bulk bias technique and % reduction in average power consumption by using bulk bias technique during write (0-50ns) and hold(50-100ns) operation.

**Fig:5.5** Average power consumed during write and read operation with and without bias technique

In Table:3, we can see that, when read operation is done after write operation the total power dissipation is reduced up to 43% by using the optimum bulk bias technique.

### 6. CONCLUSIONS

- Various leakage phenomenon’s in nano scale have been studied.
- The study of CMOS SRAM cell and various low power techniques has been carried.
- Different operations of conventional 6T SRAM cell have been studied.
- Performance parameters like Static Noise Margin of conventional 6T SRAM Cell have been analyzed.
- A 6T SRAM cell is proposed using Bulk Bias Technique.
- Average Power dissipation of proposed 6T SRAM cell has been compared with conventional 6T SRAM cells.

### REFERENCES


Author's Biography


Anurag Arora, Anurag Arora completed his BE (hons) from Apeejay college of engineering,Gurgaon and Mtech from KIIT College of Engineering,Gurgaon where, he was a gold medalist in electronics and communication branch. He has given his contributions in the area of Digital Electronics and Analog electronics. He is a member of IEEE Society; he has produced two editions of Basics of electronics Book, one edition of Microcontroller and Embedded system book, one edition of Satellite communication book and two edition of Digital Electronics book and he is also working on other books Such as Wireless communication and Digital system design.