A REVIEW OF METHODOLOGIES FOR TESTING AND LOCATING FAULTS IN INTEGRATED CIRCUITS

R. H. Khade1, D.S. Chaudhari2

1Department of Electronics Government college of Engineering, Amravati (Research scholar NMU, Jalgaon)
2Department of Electronics Government college of Engineering, Amravati

Abstract

The recent advances in semiconductor integration technology resulted in manufacturing of very large number of components on a single chip. For reliable system-on-chip, the circuit should be fault free since a single fault is likely to make the whole chip useless. Locating the faults and application of corrective measures for same chip would reduce the running cost of the system. In this paper various works related to testing and locating faults in integrated circuits is reviewed. The literature related to digital and analog integrated circuits fault is considered. Based on the literature for various fault detecting methods, the oscillation based built-in self test (OBIST) method does not require stimulus generators or complex response analyzer and it is useful in testing analog and mixed-signal integrated circuits.

Index Terms:— Built-in self-test (BIST), Circuit under test (CUT), Design for testability (DFT), Oscillation-based built-in self-test (OBIST), Path delay fault (PDF), System-on-chips (SOCs), Test point insertion (TPI).

1. Introduction

The task of finding faults in fabricated chips is highly complex and can be very time-consuming. Due to passing of faulty chips by improperly designed test, enormous difficulty in system debugging can occur. It is known that the debugging cost increases tenfold from chip to board level, and also from board to system level. Thus it is vital to detect faults at early stage. There has been a continuous pressure on VLSI chip manufacturing industry to increase the manufacturing yield. Integrated circuit manufacturers are constantly trying to decrease the number of faulty parts they produce. The reliability of System-on-Chips must be ensured to a certain extent since a single fault is likely to make the whole chip useless. Therefore, fault finding and repairing techniques are gaining importance. Manufacturer may be able to improve the circuit design or the manufacturing process by analyzing the parts that fail production tests and determine the cause of failure for each part. Detection of fault and the type of fault present in a circuit is known as fault diagnosis. With the growth of technology and advent of reconfigurable circuits like FPGAs, PLAs, CPLDs, PLDs, etc. testing only for faulty chip is not adequate. Fault location may be required to identify and then replace or discard the faulty sub-circuits. It can also be used to analyze the defect that causes the faulty behavior. Fault diagnosis is executed upon manufactured chips, which are found to be faulty in order to identify the position and types of the faults present in them. In integrated circuits various faults like electrical faults, logical faults occur and these can be due to the physical defects like defects in Silicon substrate, photolithographic defects, mask contamination and scratches, process variation and abnormalities, oxide defects. In recent years the situation has only worsened with the advent of mixed signal systems on chip (SOC), to a point where analog circuit test cost has been found to be as much as 50% of the total test cost in spite of analog portions occupying less than 5% of the chip area. As the number of MOSFETs integrated into a single chip increases, the task of chip testing to ensure correct functionality becomes complicated. However, in production environment timely delivery to customers is important. Hence a properly designed test which needs less time is necessary.

2. Types of faults present in Integrated Circuits

The various types of fault present in integrated circuits include bridging fault, stuck-at fault, stuck-open and stuck-short faults, delay fault.

Bridging Fault: In bridging faults short circuit occurs between groups of signals. This may cause an OR bridge or an AND bridge which are ones dominant or zeros dominant respectively. These faults can be found with tests used for finding stuck-at-faults. These faults can fall under the category of potentially detectable stuck-at-faults because it is not known whether a line will be pulled up or pulled down with a short at any point at time. The bridging fault will not always be detectable.

Stuck-at-fault: This fault occurs when a signal line within a circuit is permanently set to either logic high ‘1’ or a logic low ‘0’. This fault model does not have a specific cause; rather, it is an abstract fault model with numerous causes. In addition to single stuck at faults, there are situations where numerous stuck-at-faults may be in a circuit. This is called a multiple stuck-at-fault model and it can cause single stuck-at-fault tests to fail. In most situations where there are multiple stuck at faults, the faults will not mask each other and not affect the
effectiveness of a single stuck-at-fault test. If the faults do manage to mask each other the single stuck-at-fault test becomes ineffective although this is statistically unlikely to occur.

**Stuck-Open and Stuck-Short Faults:** This fault is defined as a single transistor that has either been stuck open, no current will ever pass through, or stuck short, lacking the ability to stop current. Like bridge faults, the stuck-open faults can be detected by running a sequence of stuck-at fault detection vectors.

**Delay Fault:** This fault is active when the combinational logic delay exceeds the specified clock period. The variation in the manufacturing process can cause certain portions of a circuit to be slower than other parts of the circuits causing internal signals to arrive at different times and cause functional failure. The fault is usually modelled as either a gate delay fault model where a single gate is assumed responsible for producing the slow response or a path delay fault model where certain interconnects and paths are responsible for slow propagation of a signal.

### 3. Methods of detecting and locating faults

Many researchers have worked on methods to detect and locate faults in integrated circuits. The methods of few of them are discussed here. In one of the studies the researchers used built in current sensor for $\Delta I_{DDQ}$ testing. Keating and Meyer have carried out pioneering work on $\Delta I_{DDQ}$ testing. The current consumption of the circuit changes if fault is present in the circuit and by analyzing the variation of current consumption, the faulty circuit can be differentiated from fault free one. Due to process variation the threshold voltage and leakage current varies hence instead of using absolute value, differential current is used to check the CUT. The $I_{DDQ}$ is measured indirectly by counting the clock pulses in time required to drop the voltage at disconnected node to drop below reference voltage level. The accuracy can be improved by adjusting clock frequency [1]. Test point insertion for compact test sets is evaluated by many authors. Some times the faults cannot be detected by applying test vectors. Due to such random pattern resistant faults the Built-in self-test (BIST) approach often suffers from fault coverage problem. This can be successfully improved by inserting additional logic into the CUT [2]. The test set size reduces by using Test Point Insertion (TPI) option [2][3]. Built-in self-test (BIST) technique generates test patterns and evaluates test responses inside the chip. In [4] the primitive delay faults were used. Primitive delay fault (PDF) means a path delay fault in which circuit without timing defect and all primitive delay faults are considered.

Design-for-test techniques for opens in undetected branches in CMOS latches and flip-flops have been proposed by authors [5]. In integrated circuits with high density of devices multiple metal layers are essential. These metal layers are connected by via-contacts. In such circuits there is possibility of stuck open or resistive open faults which remain undetected in some branches. By adding a small DFT circuitry, it is possible to detect both types of faults in the CMOS latches and flip-flops without much performance degradation. Das et al. have used oscillation-based built-in self-test (OBIST) methodology to test analog components in mixed-signal circuits. The OBIST method does not require stimulus generator or complex response analyzer, which makes it suitable for testing analog circuits in mixed-signal SOC environments. The frequency of oscillation depends up on the component values of the analog circuit which is to be tested. While designing stable oscillator, well defined amplitude and frequency are needed; but to test fault in CUT, it is converted to an oscillator and the variation in oscillation frequency and amplitude are used to detect the fault. The catastrophic faults arising due to various components should be modeled properly while simulating the behavior of the circuit for various faults, eg if MOSFET is stuck short then it is emulated by low resistance of value 10 Ω connected between source and drain while large resistance of value 100 MΩ is connected in series with MOSFET to emulate stuck-open fault. The fault models for MOSFET, resistor, capacitor are shown in figure 1 and figure 2 shows flow chart on OBIST method for testing procedure. The faulty circuit is detected from a deviation of its oscillation parameters with respect to the oscillation parameters under fault-free conditions [6, 7].

![Figure 1: Fault models](image)

(b) MOSFET stuck open (c) Resistor stuck short (d) Resistor Stuck open (e) Capacitor stuck short (f) Capacitor stuck open

In [8] work on detection of parametric faults in analog circuit from input/output measurements was carried out. Faults confined to passive components like resistor, capacitor and inductor are discussed. They have calculated coefficients of transfer function to detect the parametric faults and observed that there is limit in detecting small-size parametric faults in linear, time-invariant analog circuits.
4 CONCLUSIONS

This paper reviews the various methods used for detecting faults in digital and analog integrated circuits. \( \Delta \text{IDDQ} \) testing method is useful for detecting the faults. By generating a small test set the faults can be find out in reduced time. Differential measurement technique is used to find out whether the circuit is defective or not [1]. Built-in-self test approach suffer from fault coverage problem due to random-resistant faults, which can be successfully improved by means of Test Point Insertion (TPI). TPI method results in reduction of test point size [2,3]. Primitive faults due to path delay have to be tested to guarantee the performance of the circuit. By inserting a small number of control points it is possible to check the delay fault in the circuit [4]. To test resistive opens in otherwise undetectable branches in fully static CMOS latches and flip-flops a DFT technique can be used [5]. The benefit of this method is, it detects a parametric range of resistive opens with reduced performance degradation. The OBIST method does not require stimulus generators or complex-response analyzers. This method is useful in testing analog and mixed-signal integrated circuits [6].

REFERENCES


