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Ultra Low Power Hybrid Voltage Controlled Oscillator for Data Acquisition System

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Abstract: Voltage Controlled Oscillator is a predominant block in VCO-based sigma-delta analog to digital converter. A seven-stage hybrid VCO is designed to generate a high frequency of oscillation, full voltage swing, at low power consumption. The frequency of oscillation achieved for seven-stage hybrid VCO is 2.05 GHz with a low power dissipation of 144µW and output voltage swing of 1.15 V. The output noise for Hybrid VCO at 1MHz of offset frequency is 492nV/sqrt(Hz). It is pertinent to mention here that to justify the performance, robustness, scalability, and reliability worst-case analysis is considered and corner variations are performed with 500 runs of Monte Carlo simulation. The proposed hybrid VCO is designed and implemented using a cadence virtuoso platform of 0.09µm technology for a supply of 1.2V.

Keywords: Phase Noise, Output Noise, Low Power, and Eye Diagram

1. INTRODUCTION

ITRS road map has strongly suffered in technology scaling and has become a bottleneck in the realization of analog to digital and digital to analog converter. Scaled technology reduces supply voltage, intrinsic gain, output swing, dynamic parameters and increases the power consumption of analog to digital converters. With the increase in speed of wireless, wired, portable devices, and optical systems there exist a demand for high speed, low power and to improve the bandwidth of analog to digital converter [1]. In the last few years, many attempts have been made to increase the speed and reduce the power consumption of analog to digital converters by replacing the analog circuitry component with digital [2], one of the important components is a voltage-controlled oscillator based quantizer [3-5]. To design a low power, high output swing voltage-controlled oscillator-based quantizer is a way to achieve low power in a sigma-delta analog to digital converter. Voltage-controlled oscillator-based quantizer has become popular in oversampled converters due to its ease of implementation and noise shaping property [6]. Voltage-controlled based quantizer consists of voltage controlled oscillator, phase detector, and differentiator [7-8]. Although different types and topologies of oscillators exist. Two important types of controlled oscillator are 1) voltage controlled oscillator and 2) current controlled oscillator [9]. There exist different topologies of oscillators that are LC-tank VCO and ring VCO, each class of VCO has different techniques to design. one of the most popular techniques is the ring oscillator-based VCO structure. The ring voltage-controlled oscillator is of two types one is single-ended and the other differential. Single-ended ring VCO structure is shown in Figure 1.

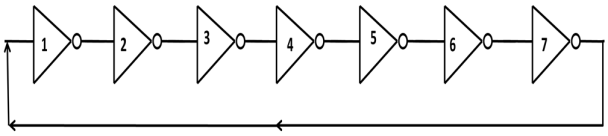

Figure 1: Single ended ring VCO structure

The frequency of the oscillation for N-stage ring VCO is expressed in eq (1).

$$f_{osc} = \frac{1}{2\, t_{delay} N} \qquad (1)$$

Where N is the number of delay elements, t_{delay} is the delay time of each element. Eq (1) implies that the oscillation frequency is inversely proportional to the number of delay element. The tdelay is completely dependent on resistance and capacitance value and is given by eq (2).

$$t_{delay} = R_{out} C_{out} \qquad (2)$$

The advantage of ring structure is the ease of integration, large tuning range, low power consumption that enables the use of oscillators in different applications. The merits and demerits of VCO existing CMOS circuits are found to have difficulties in power consumption, speed, output swing, and phase noise [10]. There exist different design of voltage controlled oscillator for different applications, but still there remains loopholes to be addressed. Table.1 shows the review of VCO's.

When it comes to design, analysis, modelling, and fabricating ring oscillators experiences difficulties and is very challenging. By considering the merits and demerits of prior work on VCO, there is a need to design low power, high output swing, and wide tuning ring VCO. In this work, focus is on design of low power, high output swing, and high frequency of oscillation using a hybrid VCO design. The workflow of hybrid VCO is described in section 2. Section 3 describes the design of low power, high frequency proposed hybrid VCO topology. The design performance is validated using the 90nm CMOS process and results are discussed in section 4. Comparison of the

proposed design with literature is discussed in section 5 and section 6 concludes the work

Table 1: literature review of voltage controlled oscillator

References	Design	Merits	Demerits
Wanching Zang *et al* [11]	Quadrature VCO	Low phase noise	More power dissipation and high design complexity
C. Sanchez-*azqueta et al* [12]	Four stage Ring VCO	Frequency of oscillation is 3.125GHz, consumes less area than LC VCO	18% of tuning range, more power dissipation.
Xioyam gvi *et al* [13]	CML Ring Oscillator	Frequency of oscillation of 2.2GHz to 2.7GHz	High power dissipation 10.1mW for a supply of 1.8V
Young seoak *et al* [14]	On chip bias current and voltage controlled ring VCO	Frequnency of oscillation 4GHz	High power dissipation of 4mW with a supply of 1.2V.
Prakash Kumar *et al* [15]	Robust current starved VCO with multiobjective revolutionary technique	Frequency of oscillation 2GHz	Power dissipation of 0.765mW for a supply of 1.8V
Jee *et al* [16]	Quadrature VCO	Low phase noise	High power dissipation, high design complexity
Abir j mondal *et al* [17]	VCO design using distict current source	Low phase noise and Low output noise	Low frequency of oscillation, power consumption of 0.786mW.
Suraj Kumar *et al* [18]	Common Source based VCO	Low phase noise, High frequency of oscillation	High power dissipation
Ricardo Martin *et al* [19]	Complementry hybrid mode VCO	High frequency of 4.2GHz	Low tuning range, complexity in design

2. WORKFLOW

The steps followed to design a hybrid VCO are represented through a flow chart as shown in Figure 2.
(a). Target specification and a new approach is chosen to design hybrid VCO to achieve low power consumption and high frequency of oscillation.
(b). Frequency of hybrid VCO is estimated using a mathematical model.
(c). Worst-case analysis, PVT variations, and corner analysis is carried out with 500 runs of Monte Carlo simulation.

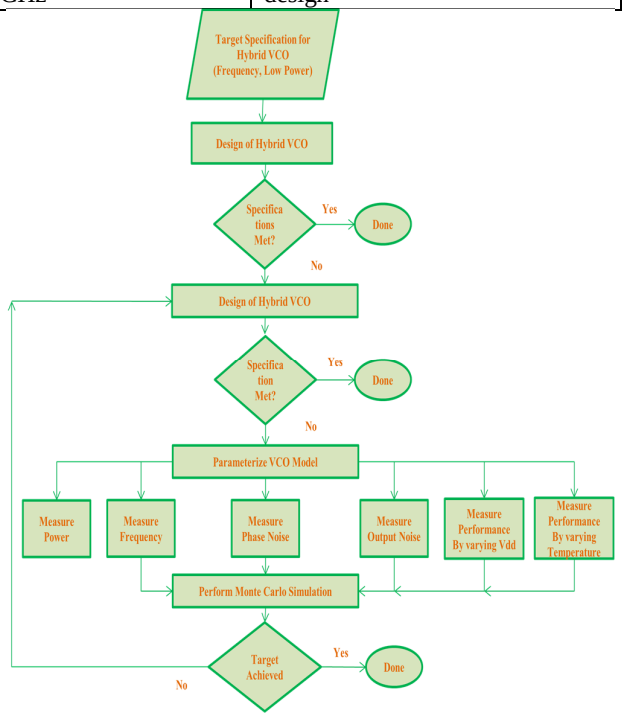

Figure 2: Flow chart of proposed Hybrid VCO

3. PROPOSED HYBRID VCO

A seven-stage hybrid VCO is designed to operate at a high frequency of oscillation and low power consumption. The

circuit diagram of the proposed hybrid VCO is shown in Figure 3. The delay cell used in designing hybrid VCO is active load common source and current starved delay cell. Active load common source delay cell is designed using PMOS(p1) and NMOS(n1) were as current starved is designed using PMOS(p2 and p3) and NMOS (n2 and n3) to bias both the delay cell biasing circuit is designed. To generate a biasing voltage (Vbias1 and Vbias2) for both the delay cell PMOS (P11) and NMOS(N12) are connected in diode-connected load.

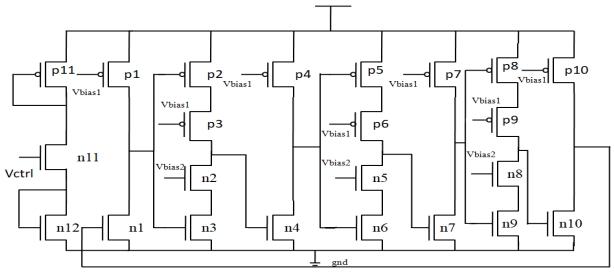

Figure 3: Proposed Hybrid VCO architecture

By varying biasing voltage the current flow in delay cell varies in turns results in a deviation of oscillation frequency, amplitude of output voltage, and DC level of oscillation. By precise design of biasing circuit frequency and amplitude can be kept large enough. To generate a high frequency of 2.05GHz device dimension of all the MOSFETs in the circuit is calculated and listed in Table. I.

Table I: Calculated Aspect ratio

MOSFET Aspect Ratio (W/L)		
N-MOSFET		P-MOSFET
N_1	W=300nm, L=100nm	P2-P10 W=120nm, L=100nm
N11	W=700nm, L=100nm	
N2, N5, N8, N12	W=500nm, L=100nm	P11 W=220nm, L=100nm
N3, N4, N6,N7, N9,N10	W=120nm, L=100nm	

The schematic of seven stage hybrid VCO is shown in Figure 4. The functionality of the design is verified using transient analysis as shown in Figure 5. Proposed Hybrid VCO is designed using a cadence platform for a supply of 1.2V. It is observed from the simulation that a stable oscillation frequency is achieved to be 2.05 GHz for a control input voltage of 1V with a output swing of 1.16V.

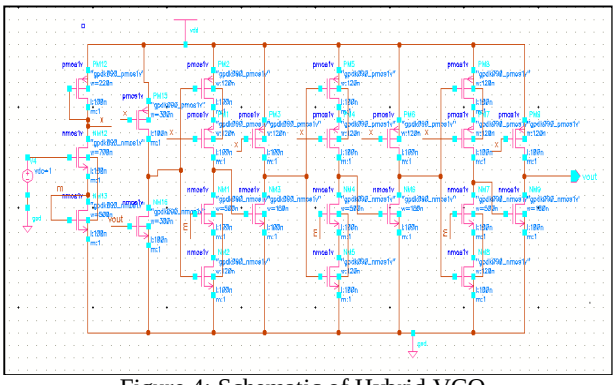

Figure 4: Schematic of Hybrid VCO

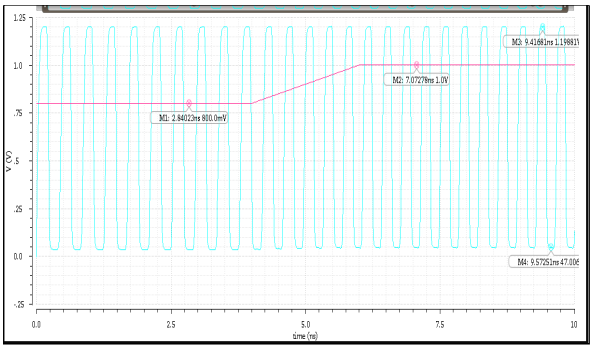

Figure 5: simulated Output Waveform of Hybrid VCO

4. MEASUREMENT AND RESULTS

Hybrid VCO is designed and analyzed on cadence 0.09µm CMOS technology. In this section, various performance parameters have been discussed.

I. Frequency of oscillation and K_{vco} Gain

For a seven-stage Hybrid VCO with input voltage Vctrl=1V the frequency of the oscillation is found to be 2.05GHz. Figure 6 shows the histogram plot for the frequency of oscillation for 500 runs of Monte Carlo. Frequency Value ranges from 1.778GHz to 2.144 GHz with a mean value of 1.9802GHz and a standard deviation of 96.35MHz.

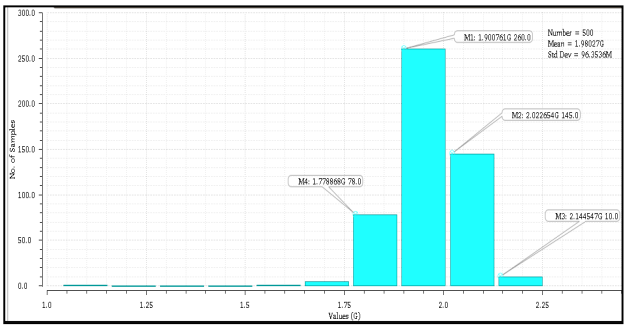

Figure 6: Histogram plot for oscillation frequency obtained from monte carlo simulation

K_{vco} is denoted as Tuning sensitivity. The ratio of variation of frequency of oscillation with a variation of control voltage is termed tuning sensitivity. Figure 7 shows the variation of Kvco with Vctrl. It is also observed that as

tuning sensitivity increases with the increase of supply voltage. Tuning sensitivity increases as control voltage increases to 0.8V. After 0.8V the tuning sensitivity decreases.

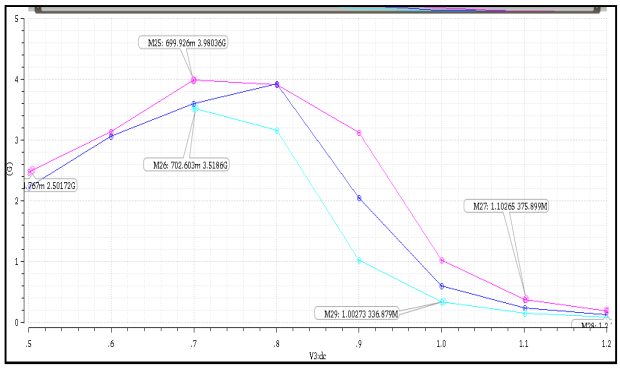

Figure 7: simulated and Measured Kvco Gain Vs control voltage

II. Analysis on control voltage

Deviation in oscillation frequency as a function of control voltage is shown in Figure 8. It is observed that frequency of oscillation is directly proportional to control voltage Vctrl. Figure 9 shows the variation of frequency as a function of control voltage and temperature. At -27°C the frequency of oscillation is 2.624GHz and reduces to 1.64GHz at 97°C.

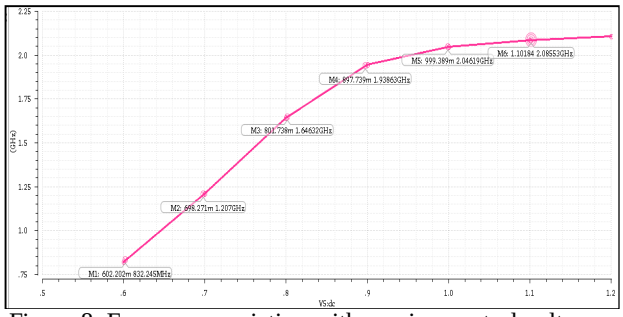

Figure 8: Frequency variation with varying control voltage

On increasing the temperature the frequency of oscillation decreases. Figure 10 displays the frequency variation as a function of control voltage and supply voltage. From the obtained results the frequency of oscillation is directly proportional to supply Voltage. For supply of 1V frequency is 1.5GHz and Increases to 2.61GHz for the supply of 1.2V.

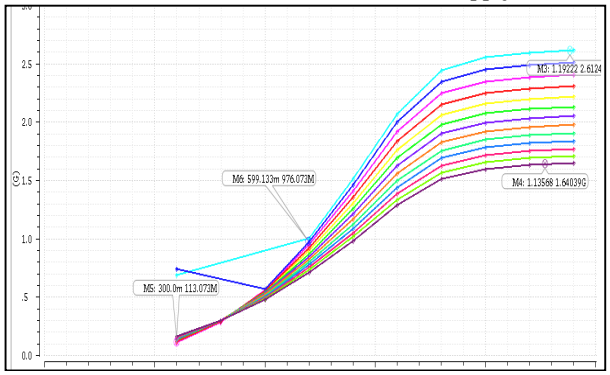

Figure 9: Output frequency with varying Temperature

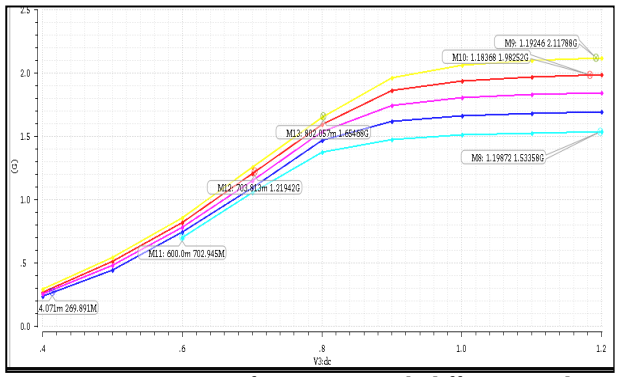

Figure 10: Variation of Frequency with different supply voltage

The histogram plot for average power for 500 runs of Monte Carlo is shown in Figure 11. The mean value of average power is found to be 142.19µW with a standard deviation of 7.61µW.

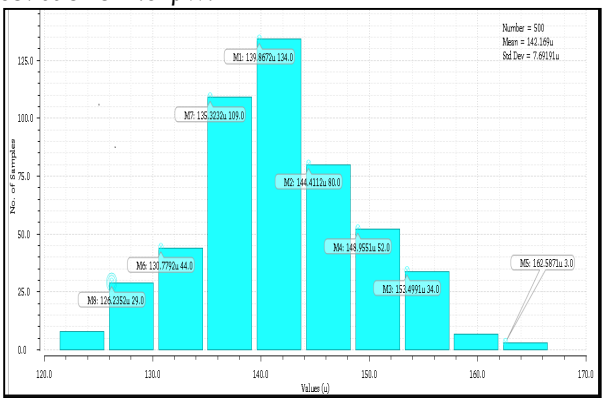

Figure 11: Histogram of average power obtained from monte carlo simulation.

III. Eye Diagram

Jitter and output voltage margin is the important parameter of VCO. For an ideal oscillator, the spacing between two transitions is constant, when it comes to the practical application of VCO it varies. This uncertainty is called Jitter, it increases with an increase in the simulation time interval. Eye height determines the output voltage and Eye width determines Jitter. Eye height for the Hybrid VCO is found to be 1.148V. The jitter of the proposed Hybrid VCO is found to be 47ps p-p as shown in the eye graph in Figure 12. The clear voltage of Logic 0 and Logic 1 is found to be 49.25mV and 1.1976V respectively.

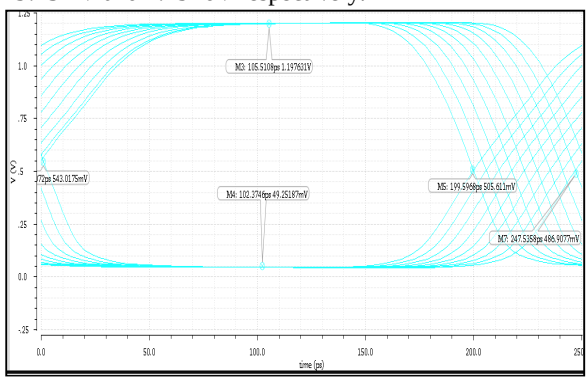

Figure 12: Simulated eye diagram for Hybrid VCO

IV. Johnson noise

Johnson noise is one of the key concerns of Hybrid VCO and filtering is a tedious process. The plot between Vn *Vs* frequency is shown in Figure 13. The noise plot is shown for the variation of V_{dd}. It is observed when the supply voltage V_{dd} is increased Johnson noise increases. The output noise saturates after 2 kHz. At the magnitude of 2GHz, the noise is found to be 492nv/sqrt(Hz).

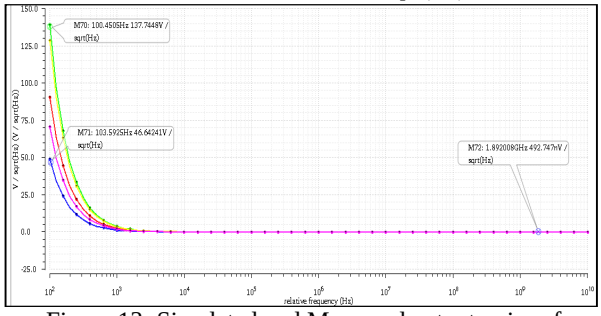

Figure 13: Simulated and Measured output noise of proposed Hybrid VCO

V. Phase Noise

Phase noise is one of the important properties of ring VCO. It is the ratio of noise with the power of the carrier signal. The phase noise is denoted as L (Δf) for ring VCO [20] is expressed as

$$L(\Delta f) = \frac{3}{8n}\frac{kbT}{p}\frac{vddf^2(osc)}{vchar\,\Delta f^2} \qquad (2)$$

Were kbT= Boltzmann constant, T= room temperature, P= total power dissipation, Δf =offset frequency. At 1MHz offset from the oscillation frequency, the phase noise of hybrid VCO is -76.3dBc/Hz is shown in Figure 14.

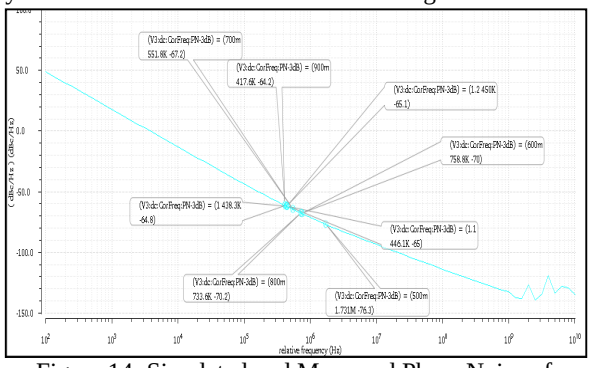

Figure 14: Simulated and Measured Phase Noise of Proposed Hybrid VCO

VI, Best/Worst Case Analysis

To examine the best case and worst case analysis hybrid VCO experience simulation in FF corner for the best case and SS corner for the worst case. The obtained result for hybrid VCO is summarized in Table II. Table II shows the variation of average power and frequency of oscillation for different process corners. The performance of average power and frequency of oscillation is established to stay unchanged from zero skew to 5% Process Skew. It is found the average power altered through the simulation at the nominal corner is changed by 37.06%, 12%, 9%, and 28.2% in SS, SF, FS, and FF corner respectively. Table III shows the variation of a metric against the PDN effect. Power delivery network (PDN) consists of inductance, resistance, and capacitance offered by printed circuit board, pin, package, and power supply variation.

5. PROPOSED HYBRID VCO

To determine the overall performance of hybrid VCO we have compared performance parameters such as average power, frequency of oscillation, and phase noise shown in Table IV. From Table IV it is observed from the previous existing circuits achieved excellent oscillation frequency at the cost of higher power dissipation making the circuit more vulnerable for high-speed SOC devices. The proposed Hybrid ring VCO structure not only increases the frequency of oscillation it also reduces the power dissipation of the circuit drastically. Proposed Hybrid VCO cell reduces power dissipation of 94.28%, 98.86%, 98.59%, 99.59%, 81.42%, 53.72%, 99.13%, 87% and 94.30% when compared to [21-30] also increases oscillating frequency of 49.75%, 6.34%, 48.78%, 82%, 76.58%, 78.08% and 32.68% when compared to [21,22, 24-30]. Overall the Hybrid VCO achieves ultra-low power with a high frequency of oscillation.

6. CONCLUSION

A low-power, high-frequency seven-stage hybrid voltage-controlled oscillator is designed and analyzed. The frequency tuning range of VCO is from 523MHz to 2.08MHz for varying control input voltage from 0.4V to 1.2V and its phase noise is -76.3dBc/Hz at 1MHz offset frequency. The Hybrid VCO is implemented in 90nm CMOS technology with a power burn of 144µW for a supply of 1.2V. VCO exhibits superior performance in terms of output voltage, low power consumption and frequency of oscillation. The measurement result validates that a stable VCO can generate a stable frequency for VCO-based Converter application.

Table II: Worst case and best case analysis of frequency, average power @ with and without skew

	Process Corner	No Skew		5% Process Skew				Frequency Range
		Power (µW)	F_{osc} (GHz)	Power (µW)		F_{osc} (Hz)		
Pre Layout				X	Σ	X	Σ	
	NN	143.2	2.05	146.47	8.48	2.03G	89.43M	523MHz -2.08GHz
	SS	90.47	1.35	93.635	6.13	1.305G	63.842M	702MHz – 2.2GHz
	SF	125.4	1.76	130.87	11.90	1.74G	105.3M	500MHz – 1.98GHz
	FS	129.5	1.975	131.264	6.25	1.921G	69.09M	692MH – 2GHz
	FF	200.6	2.815	205.831	11.4	2.749G	112.879M	488MHz-2.8GHz

Table III:Deviation of frequency and average power against PDN effect

Parameter	NN Corner (zero variation)	10% Variation in VDD
Oscillation Frequency (GHz)	2.05	1.88
Average Power(µW)	143.2	70.1

Table-IV: Performance comparison of Hybrid VCO

Parameters	Proposed work	[21]	[22]	[23]	[24]	[25]	[26]	[27]	[28]	[29]	[30]
Supply Voltage	1.2	1	1.8	1.8	1.8	3.3	0.6	1	1.2	1.5	1
Average Power (mW)	0.143	2.5	12.6	10.2	10	35.5	0.77	0.309	7.68	1.1	2.51
Oscillation Frequency (GHz)	2.05	1.03	1.92	2.2	1.05	0.369	0.480	0.450	3	1.38	3.47
Technology	90	180	180	180	180	180	90	90	65	40	60
Phase Noise at 1 MHz	-76.3	-105	-91	-89	-102	-88	-89	-105	-94	-98	-98.

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