DESIGN OF 16 BIT HIGH PERFORMANCE DIGITAL CMOS PARALLEL COUNTER USING STATE PREDICTION LOGIC

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Abstract: We present a parallel counter design that achieves high operating frequencies and consumes less power through a novel pipeline partitioning methodology. This is proceeded to eliminate the carry chain delay and reduce AND gate fan-in and fan-out. Here only three simple CMOS logic modules are used. These three modules are placed in a highly repetitive structure in both the counting path and state look-ahead path. An initial module generates anticipated counting states for higher significant bit modules through the state look-ahead path. The main advantage of our counter include power in milliwatt(mw) range and speed in the range of GHZ. The design is implemented using Microwind, digital schematics (DSCH) and 0.12µm technologies. Performance shows a total power consumption of mw with a operating frequency of GHZ.

Keywords: counting path, state look ahead logic, digital circuits, counting state, state equations.

1. INTRODUCTION

Counters are used in almost all digital circuit and systems such as frequency synthesizer, measuring systems, analog to digital converters, counters are also used as a basic building blocks for more advanced digital systems. High speed parallel counters find numerous applications for arithmetic operations that include neural networks and triggering the nuclear instruments. digital systems. The key features required will vary greatly depending upon a particular Early design methodologies improved counter operating frequency by partitioning large counters into multiple smaller counting modules, such that modules of higher significance (containing higher significant bits) were enabled when all bits in all modules of lower significance (containing lower significant bits) saturate. Initializations and propagation delays such as register load time, AND logic chain decoding, and the half incremener component delays in half adders dictated operating frequency. Subsequent methodologies improved counter operating frequency using half adders in the parallel counting modules that enabled carry signals generated at counting modules of lower significance to serve as the count enable for counting modules of higher significance, essentially implementing a carry chain from modules of lower significance to modules, counting modules of higher significance contained more cascaded carry-ripple adders than counting modules of lower significance. Each counting module's count enable signal was the logical AND of the carry signals from all the previous counting modules (all counting modules of lower significance), thus pre scaling clocked modules of higher significance using a low frequency signal derived from modules of lower significance. Due to this pre scaling architecture, the maximum operating frequency was limited by the incremener, DFF access time, and the AND gate delay. The AND gate delay could potentially be large for large sized counters due to large fan-in and fan-out parasitic components. Design modifications enhanced AND gate delay, and subsequently operating frequency, by redistributing the AND gates to a smaller fan-in and fan-out layout separated by latches. However, the drawback of this redistribution was increased count latency (number of clock cycles required before the output of the first count value). In addition, due to the design structure, this counter architecture inherited an irregular VLSI layout structure and resulted in a large area overhead.

2. PARALLEL COUNTER DESIGN

The architecture of our high speed parallel counter width is shown in figure 1. The figure 1 clearly shows the counting path circuits is partitioned into uniform synchronous 2 bit parallel counter respectively in sequence and the state look ahead logic path consists of 2 input and gates and three input and gates and inverters. Counting path logic performs the counting of states while the state look ahead logic circuit indicates early overflow signals, which are required by the counting path for proper working of the counter. A common clk and reset signals are connected to both paths which finally results in a synchronous working type of counter. The figure 1 shows clearly shows the counting path which consists of three different circuit blocks as indicated in labels.
Module 2 is acting as a pipelining structure between module 1 and module 3 and then subsequently between successive module 3s. In state look ahead path, each states of module are selected and subsequently pipelined. This is used for enabling the module 3s and the level of pipelining is depending upon the module 3s position in the counting path. For enabling ith module3 in the counting path ,we need to generate the enabling signal from state look ahead path up to the (i-1)th module 3 Counting path.

Figure 1: 16 bit counter of module 1 and module2 and module 3.

A detailed circuit diagram of module 1 is shown in figure 2. module 1 is a standard parallel synchronous binary 2-bit counter, which is responsible for low order bit counting and generating future states for all module 3s in the counting path by pipelining the enable for these states future states through the state look ahead path. From Module 1,outputs Q0 and Q1 are taken directly as the LSBs and an additional output EN1 is also generated from this circuit which is used as enabling signal subsequently. The EN1 is given as the input to the module 2,all the two outputs are used for selection of the early overflow states. In the state looks ahead path circuit. Depending upon the number of output bits of module 1, the overall width of the counter can be increased to any number of bits. Circuit diagram of module 2 is shown in figure 3. It is a simple D flip flop and it acts a delay element in the circuit. Module 2 is used in both the counting path and state look ahead path. In counting path, the output of the module 2 is a given a enabling signal INS to module 3,thus it can be seen that in counting path,module2 is pipelining the enable signal of module 3s and in state look ahead path, pipelining the early overflow states.

Figure 2: MODULE

Circuit diagram of module 3 is shown in figure 4.it is a synchronous 2 bit parallel counter. Module 3 produces its outputs Q0 and Q1,which forms the MSBs of the counter. Also an additional output EN3 is generated by anding its output with qc signal, which is generated by the state look ahead logic path. The signal ins is again pipelined by module 2 and I given as input to next module. he overflow states of each block are predetermined and the output states of module 1 are decoded, in other words it means selecting a particular output state to enable a particular module by the addition of appropriate number of delay elements. The state look ahead path circuit selects different states of module 1 and then introduces suitable delays or pipelines those states depending upon the order of module 3 in the counting path. For this the enable supporting signals are required to be generated. To enable the highest order blocks in the counter design, the repeated delaying and performing adding operations of the selected states of module 1 is required. The state look-ahead path operates similarly to a carry look-ahead adder in that it decodes the low-order count states and carries this decoding over several clock cycles in order to trigger high-order count states. The state look-ahead logic is principally equivalent to the one-cycle look-ahead mechanism in the counting path.

Figure 3: Module 2

Figure 4: Module 3

For example, in a 4-bit counter constructed of two 2-bit counting modules, the counting path’s module-2 decodes the low-order state Q1Q0=10 and carries this decoding across one clock cycle and enables Q3Q2=01 at module-3 1 on the next rising clock edge. This operation is equivalent to decoding Q1Q0=11 and enabling Q3Q2=01 on the next immediate rising clock edge. The state look-ahead logic expands this principle to an X cycle look-ahead mechanism. For example In a traditional 6-bit ripple counter constructed of three 2-bit counting modules, the enabling of bits Q5Q4 happens only after decoding the overflow at Q1Q0 to enable Q3Q2 and decoding the overflow at Q3Q2 to enable Q5Q4.
However, combining the one cycle look-ahead mechanism in the counting path for Q3Q2=10 and a two-cycle look-ahead mechanism for Q1Q0=01 from can enable Q5Q4 Q1Q0=01 is pipelined across one cycle, thus enabling Q5Q4 at the rising clock edge (further details will be discussed in section II-C). Thus, enabling the next state’s high order bits depends on early overflow pipelining across clock cycles through the module-2s in the state look-ahead path. This state look-ahead logic organization and operation avoids the use of an overhead delay detector circuit that decodes the low order modules to generate the enable signals for higher order modules, and enables all modules to be triggered concurrently on the clock edge, thus avoiding rippling and long frequency delay Circuit operation.

3. COUNTER STATE EQUATION:
By using early overflow pipelining equations, the counter state equations can be easily derived. It is known that for enabling the count states Q16 and Q15 which are current count states, the state equation must contain q14, q13,...q1 which are the past count states. We have derived 16-bit state equations by starting from 4-bit counter state equations.

Q4Q3Q2Q1= Q4Q3pipelined (q1-2 q1-1) - For 6-bit counter state equation
Q6Q5Q4Q3Q2Q1= Q6Q5pipelined [(q4q3) pipelined(q1-3 q1-2 q1-1)] - For an 8-bit counter state equations may be given by
Q8Q7Q6Q5Q4Q3Q2Q1= Q8Q7pipelined [(q6q5) pipelined [(q4q3) pipelined(q1-3 q1-2 q1-1)]].(3)
For 10-bit counter state equation are given as follows
Q10Q9Q8Q7Q6Q5Q4Q3Q2Q1= Q10Q9pipelined [(q8q7) pipelined [(q6q5) pipelined [(q4q3) pipelined( q1-3 q1-2 q1-1)]].(4)
For 12-bit the state equations are
Q16Q15Q14Q13Q12Q11Q10Q9Q8Q7Q6Q5Q4Q3Q2Q1= Q16Q15 pipelined [q14q13pipelined (q12q11) pipelined [(q10q9) pipelined [q8q7] pipelined[(q6q5) pipelined[(q4q3) pipelined ()]]].(7)

4. DESIGN OF A CLOCK
In this subsection, we analyze the area overhead of our parallel counter architecture based on the number of internal components (which can easily be translated to gate counts). Module-1 is a 2-bit counter that provides a set of early overflow states to enable future states. In general, if module-1 is a 1-bit counter, one early overflow state inputs into the counting path and the remainder of the early overflow states input into the state look-ahead path. Therefore, the total number of early overflow states (EO) generated by module-1 is
EO= 2^n-1
For proper working, path delays of counting path and state look-ahead path should be less than the clock period of the counter. Here assuming that access time for both module 1 and module 3 are essentially equal. Let T clock be the clock period of the counter, T module be the access time of block circuits module1 or module3, T3-AND be the gate delay of 3-input AND gate, Ts be the combined set-up time and hold time of D flip-flop. For proper working, path delays of counting path and state look-ahead path should be less than the clock period of the counter [1]. Here assuming that access time for both module 1 and module 3 are essentially equal. Let T clock be the clock period of the counter, T Block be the access time of module1 or module3, T3-AND be the gate delay of 3-input AND.
Tclock > Tmodules + T3-AND + Ts
The clock period mainly depends on the block access time. Hence, for any changes in the design like increasing the number of output bits of the blocks or using different D flip-flops the clock period will change substantially. This condition is very stringent and must be kept in mind while designing the circuits or block for fast counters. In this research work, clock is designed while keeping various delays in mind.

5. SIMULATION RESULT ANALYSIS
The performance of the high speed parallel counter is verified by simulating the circuit with wide range of output conditions. The tools used for carrying out simulation tests are mainly based on software from microwind and digital schematic DSCH. Microwind is electronic design automation software which diagrams integrates very conviently the front end and the back end of the chip design principles of vlsi .it is possible to generate the layout of the circuit in microwind either by using verilog code file of the circuit design or by directly using schematic layout. it is also possible to measure the area utilized by the circuit design by using microwind software. during this research DSCH is mainly used for
the design of circuit schematics and for generating timing waveform

**TABLE1. SUPPLY VOLTAGE AND POWER CONSUMPTION**

<table>
<thead>
<tr>
<th>Technology (µm)</th>
<th>Supply voltage (v)</th>
<th>Power (mw)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.12</td>
<td>1.2v, 2.5v</td>
<td>0.443</td>
</tr>
<tr>
<td>0.6</td>
<td>5v</td>
<td>63.112</td>
</tr>
<tr>
<td>0.8</td>
<td>5v</td>
<td>65.21</td>
</tr>
<tr>
<td>1.2</td>
<td>5v</td>
<td>83.565</td>
</tr>
</tbody>
</table>

Power estimation we simulated a 16-bit counter circuit which was designed using microwind3.1.it produced encouraging results. the clock frequency of 1 GHZ is chosen for the simulation test and verification. the total power consumed by the counter circuit under different technologies is compiled

**TABLE2: TRANSISTOR COUNT AND AREA REQUIREMENTS ON CHIP FOR 8 AND 16BIT COUNTERS**

<table>
<thead>
<tr>
<th>Counter bit size</th>
<th>Transistor count</th>
<th>Area (µm²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>8</td>
<td>370</td>
<td>4699</td>
</tr>
<tr>
<td>16</td>
<td>1199</td>
<td>8848</td>
</tr>
</tbody>
</table>

6. TIMING WAVEFORM DIAGRAM ANALYSIS

The timing waveform diagram of simulation tests of the high speed parallel counter is shown in figure. It has been clearly observed that there are fluctuations in timing waveforms of the counter at various levels of the signals. from timing waveform it can be clearly observed that least significant bits are subjected to more fluctuations compared to least significant bits. We simulated the 16-bit circuit with constant clock frequency of 1GHz for various technologies. Table 1 show the variation in power for various technology used while simulating the tests. From the Table 1, it can be verified that while designing at lower technology values (reducing the size of channel length) there can be considerable reduction in power consumption. Our simulation results show that if the technology used is reduced in size by a factor of 10, the power consumption reduces by a factor of roughly over 500 times. The power consumption initially reduces with a slow rate, but as the technology size reduces further the power consumption reduces exponentially faster and faster. Our simulation results are carried out on an average accuracy software and hardware.

7. CONCLUSION

In this paper we have reported the concluding analysis and results of our simulated design and verifications on a scalable high-speed parallel counter. We have subsequently tested and verified design starting from 8-bit to 16-bit count size. The special features of this counter design which have emerged out of testing and verification process include the modularity and pipelining structure. One can implement counter of any larger numbered bit size without needing much complexity and design efforts due to the nature of the modularity of design. To achieve this, we only need to have module3 and module2 in appropriate numbers at appropriate positions in order to design a desired larger bit width counter. Positioning of module2 (D flip-flops) has much more bearing in the counter design and subsequently its performance. The introduction of module2 has resulted in exclusion of AND gates with large fan-in for the enabling of higher order count bits. This is clearly observed as an advantage. After attaining the maximum count of a given design, if it is required to further increase the counter width, it can be done simply by increasing the counter width of module1. Since all the circuit blocks except module1, of counting path are preceded by module2 (D flip flop), therefore, all the circuit blocks will be getting enabled with constant delay. Hence there is no mismatch of delays. Since the counter is having binary output, there is no need of any detector circuits at output. The result analysis shows some of the important findings in terms of transistor count and chip area requirements. The transistor counts have shown very comparable results available for literature review. Some rough patterns have emerging for the possible relationship between transistor count, power consumption and technology size. These findings may result in very concrete physical laws and principles if verified with higher precision and accuracy involved with the software tools used for implementation. The future work will involve further refining the results and improved designs of more complex circuits and systems.

**FIGURE 6. OUTPUT WAVEFORM**
REFERENCE:


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