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High-Performance Low-Cost Image Processing Unit for Small Satellite Earth Observation using COTS Devices

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Abstract: ***Earth observation is one of the most important applications of space systems. The ability to realize earth observation using small satellites enables cost-efficient earth observation. To do this, improvements are inevitable for high-performance image processing units. We developed a high-performance image processing system for earth observation, HP-IMAP-EO, using commercial off-the-shelf technologies. To achieve good reliability against radiation effects, an autonomous hierarchical monitoring system is introduced. We planned to install HP-IMAP-EO on three satellites, TSUBAME, ChubuSat, and Hodoyoshi-3, which are scheduled for launch in 2014. In this paper, we introduce the outline of HP-IMAP-EO and the strategy used to achieve high reliability to counter radiation effects.***

Keywords: Earth Observation, Image Processing, COTS Devices, FPGA

1. INTRODUCTION

Earth observation is one of the most important applications of space systems. Wide-area images acquired by space systems can be utilized for various types of applications such as disaster monitoring [1]-[2], and vegetation monitoring [3]. Various types of earth observation satellites are currently utilized and are scheduled for launch.

Meanwhile, there has been significant interest in the use of small satellites to reduce the cost of space systems [4]-[7]. Small satellites enable a reduction of both the development and launch costs, because the structure of small satellite systems is relatively simple than that of full-scale satellites, and small satellites can be launched as auxiliary payloads. If we realize earth observation using small satellites, we can achieve more cost-efficient earth observation, considering the high demands for its services.

To realize earth observation using small satellites, significant improvements are inevitable for existing high-performance image processing units. Generally, the data transmission bandwidth of a small satellite is limited; the resolution of an observation sensor has remarkably improved. It is difficult to directly receive acquired high-resolution image data on downlink, and the data therefore need to be processed and stored on board the satellite. Therefore, we need a high-performance on-board image processing system that also possesses the ability to store a large amount of data. Because the size and weight of the satellite are also limited, the image processing system needs to be as small and lightweight as possible.

Current space cameras are large and costly, because priority is usually placed on ensuring component reliability in space. Their processing capabilities are also limited, because they require highly reliable and conservative devices. Although devices for terrestrial applications are continually being improved, limited progress has been made with devices that need to be sufficiently reliable for use in the harsh environment of space. However, if the use of devices for terrestrial applications is possible for space activities while maintaining high performance, the development costs can be significantly reduced. We have previously applied commercial off-the-shelf (COTS) technologies and experimentally verified the suitability of advanced devices and technologies in several space missions [7]-[13]. Based on these experiences, we developed a very small, high-performance image processing unit based on COTS technologies with a calculation capability of 500 million instructions per second (MIPS) on a single 50 mm × 50 mm printed circuit board, and which incorporates various interfaces using field-programmable gate array (FPGA) technology [11]-[13]. Using this image-processing unit, we developed a small, low-cost camera with image processing capabilities for spacecraft applications. The camera is called the high-performance image acquisition and processing unit (HP-IMAP). HP-IMAP technologies have been successfully demonstrated on the Interplanetary Kite-craft Accelerated by Radiation of the Sun (IKAROS) spacecraft, which was launched on May 21, 2010. The mission of IKAROS is to evaluate the performance of solar power sails, which are large membranes that use sunlight for propulsion [13].

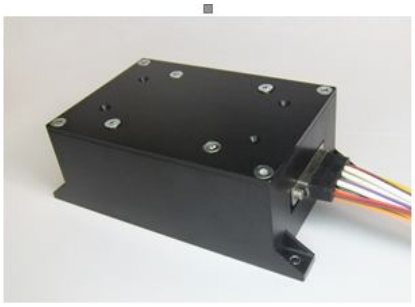

Fig. 1: High-Performance Image Acquisition And Processing Unit For Earth Observation (HP-IMAP-EO)

HP-IMAP is mainly focused on image processing for relatively low-resolution situation monitoring. By expanding the performance of HP-IMAP, we develop a high-performance image processing system for earth observation, called HP-IMAP, for earth observation (HP-IMAP-EO). To satisfy the requirements for high-data transmission rate and the large data capacity of earth observation, the FPGA was upgraded from VertexIIpro to Vertex4FX (Fig. 1). Based on the FPGA upgrade, there are concerns that the occurrence of radiation effects such as single-event effects (SEEs) will increase, because the effects of single events are a probabilistic effect caused by the interaction between radiation particles and logical elements, and the probability tends to increase for a higher density of logic elements.

To achieve high reliability against radiation effects, a hierarchical monitoring system was adopted. The watchdog timer of the FPGA observes task-level anomalies and evokes a mild task reset to maintain the function of the processing system. In addition to the internal watchdog timer, a programmable IC is installed as an external watchdog timer to prevent cases in which the FPGA cannot recover itself. The PIC has limited calculation capabilities, but the single-event probability is quite low, because the density of the logic elements is very low. The over-current situation caused by the single-event latch-up (SEL) can be detected by a non-logical current detection and reset circuit. Based on radiation test experiments, it was confirmed that radiation effects can be successfully mitigated using an autonomous hierarchical monitoring system (Fig. 2).

Now, HP-IMAP-EO is scheduled to be installed in three satellites, TSUBAME, ChubuSat, and Hodoyoshi-3, which are scheduled for launch in 2014. In this paper, we introduce the outline of HP-IMAP-EO and the strategy employed to achieve high reliability against radiation effects.

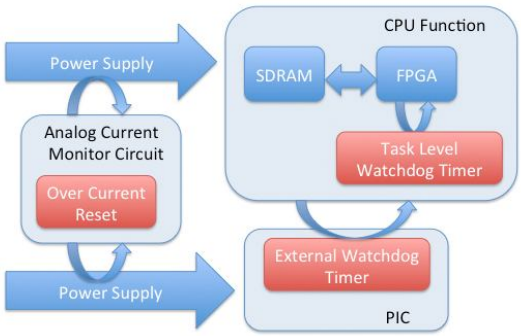

Fig. 2: Concept of Hierarchical Monitoring System

Table 1: Specifications of HP-IMAP-EO

Processor	powerpc405@400MHz
DRAM	DDR2SDRAM 256MByte
SPI Flash memory (BOOT)	8MByte
NAND Flash memory (Program and Data store)	2GByte
SDCard（Data store）	2GByte × 2
insulated RS-422	115.2kbps
RS232C	115.2kbps
Ethernet	10BASE-T/100BASE-TX
CAN2.0B	1Mbps
Power Supply	unstable 24V(19-32V) comsumption Max.5.5W Typ.4.5W
Operating temperature	0～60℃
Storage temperature	-25℃～85℃
size	110mm × 60mm × 35mm
mass	Less than 200g

2. HIERARCHICAL MONITORING SYSTEM AGAINST POSSIBLE ANOMALIES CAUSED BY RADIATION

2.1 Radiation Effects on the Electronics Devices

In the spacecraft's orbit, solar radiation and particles emitted by the Sun can directly affect on-board electrical devices. The radiation effect is a key difference between the terrestrial environment and the orbital environment.

The radiation effect can be divided into two categories: the total ionizing dose (TID) and the SEE. The TID is an irreversible degradation effect caused by a large amount of radiation. This effect significantly depends on the material and fabrication process of the devices, and it corresponds to the potential lifetime of the devices in the orbit. The TID can be verified by the gamma radiation test, and the validation and screening of the devices are therefore considered to be effective measures.

The SEE is a probabilistic effect caused by the radiated particles, and the major effects are the single-event upset (SEU), which causes the bit inversion of logical devices and memories, and the SEL, which causes a tentative over-current condition. Generally, the SEL can be recovered by a rapid power reset of the devices; therefore, a good approach for the mitigation of the SEE is to detect the SEL by taking the current measurement and evoking the power reset. The effect of the SEU is highly logical and occurs in a probabilistic manner, based on the characteristics measured by the particle radiation test.

2.2 Mitigation of Single-Event Latch-up Effects

The probabilistic level of an SEL is quite low, but it cannot be negated, because it causes permanent failure if it is not properly treated. Because it is easy to recover from an SEL by performing a hard reset, namely tentative power off situation, the problem is how to detect the SEL and to perform a secure reset. Because the SEL causes a high electric current in the power line, the current detection and reset circuit is installed in the power conversion units. Because the logical elements may themselves cause the single event, the reset circuit should consist of analog and very low-level logic elements.

2.3 Mitigation of Single-Event Upset Effects

The SEU, which refers to bit flipping, causes software anomalies. With respect to the mitigation for memory elements, the implementation of an error correction system by redundant memory coding should be the most direct way to mitigate against an SEU [8]. However, the utilization of an error correcting bit highly suppresses the memory capacity. In the case of high-memory-requirement applications such as image processing in earth observation applications, such a suppression of memory usage is critical. Moreover, redundant coding suppresses not only the memory capacity but also the logic element usage in the case of the FPGA.

Therefore, the use of a functional error detection and mitigation process, such as a watchdog timer, is needed for HP-IMAP-EO, but for safety considerations, the watchdog timer is installed in a hierarchical manner. First, each task is monitored by a specific watchdog process. If any anomalies are detected in this process, the milder mitigation process, i.e., a task level reset, is evoked. The effect of this level reset is limited and marginally affects the function of the entire system. However, anomalies may occur at any point, and the watchdog process itself may be affected by the single event or by other effects. In the case in which the mitigation process for task-level anomalies is suspended, the external watchdog timer is adopted using a programmable IC (PIC). The PIC has limited calculation capabilities, but the single-event probability is quite low, because the density of the logic elements is very low. The PIC monitors only the FPGA anomalies and evokes a hard reset in the case of anomalies to refresh all memory areas, including the operating system (OS) area.

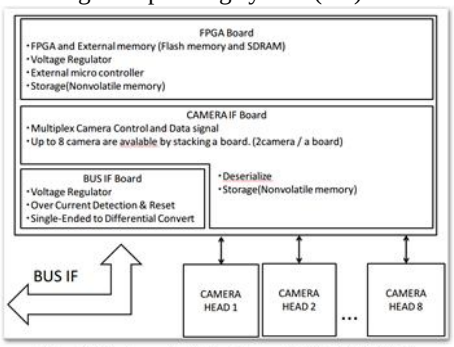

Fig. 3: System Architecture of HP-IMAP-EO

3.HIGH-PERFORMANCE IMAGE ACQUISITION AND PROCESSING UNIT FOR EARTH OBSERVATION (HP-IMAP-EO)

HP-IMAP-EO has two camera interfaces that acquire 8 megapixel class image data. Its size is 110 by 60 by 37, and its weight is less than 200 g. The major specifications of HP-IMAP-EO are summarized in Table 1.

HP-IMAP-EO consists of three boards: the FPGA board, the bus interface board, and the camera interface board. (Fig. 3)

3.1 FPGA Board

The most significant feature of this board is that the high-performance FPGA, including the CPU IP core and its peripherals such as RAM and flash memory, is realized on a very small board (47 mm × 47 mm). (Fig. 4)


Fig. 4: FPGA Board

Furthermore, by utilizing the reconstruction function of the FPGA feature, it is very easy to expand various types of interfaces and functions. Actually, by using such a capability, the same unit is used in various earth observation missions of Hodoyoshi-3, TSUBAME, and ChubuSat.

The main components of the FPGA board are shown below:

- Virtex4FX (FPGA)
- PIC24HJ (Microcontroller)
- LAN8700 (Ethernet PHY)
- M25P64 (Serial flash memory)
- MT47H (DDR2 SDRAM)
- Micro SD Card connector
- EN53xx Regulator
- MCP9800 (temperature sensor)
- FX6-40 Connector x 2

Virtex4FX has a PowerPC processor (PPC405) and a media access controller (MAC) by hard macro. PPC405 is

driven at 450 MHz at the maximum, and it is sufficiently fast to realize data acquisition and image processing for earth observation applications. Virtex4FX has a sufficient number of logic elements to realize major interfaces, enabling earth observation applications, but in the case in which the user is expected to utilize a larger number of logic elements to achieve very complicated interface logic, it can be improved by connecting an auxiliary processor (APU) by fabric coprocessor bus (FCB) of PPC405. The board includes a 128 MByte SDRAM and an SD card, in addition to an 8 MByte serial flash memory, which is used for the storage of software libraries. An EthernetPHY IC is installed for mainly debugging purposes, but it can be utilized in future applications in which an Ethernet connection is supported by the satellite's on-board computer. PIC24HJ is used for situation monitoring as a part of the autonomous hierarchical monitoring system that is mentioned above. The FPGA board is designed to provide an interface to other extension boards such as the camera interface board through two of the FX6-40 connectors that interconnect boards in a gap of only 5 mm.

3.2 CAMERA IF Board

The camera interface (IF) board is one of the extension boards of the FPGA board, and it covers the interface with various types of camera head. (Fig. 5) Image data, including a clock-synchronized parallel data stream, are captured and automatically stored in the SDRAM of the FPGA board using direct memory access through the bus connection. The camera interface also covers the serialize and de-serialize interface capabilities in the case in which it is expected that the camera head will be installed at some distance from the processing unit, since the serial interface is very robust to the length of the interface cable. The camera interface de-serializes the signals, which are the serialized pixel clock and the pixel data in the camera head unit. This function is covered by a complex programmable logic device (CPLD).
In the case in which the camera head interface is changed, the camera interface board is customizable, and the FPGA board can be utilized in the same structure.

Fig. 5: Camera Interface Board

In addition to such basic functions, the camera interface board covers additional functions such as data storage using 2 GB NAND flash memory and debug interfaces using JTAG, RS232C serial, and Ethernet.

3.3 BUS IF Board

The interface functions, such as the power interface, telemetry and command interfaces, are covered by the bus interface board. In the case in which the satellite interface changes, the bus interface board is customizable, and the FPGA board and camera interface board are free from modifications. (Fig. 6)
The BUS IF board has a regulator from 5 V to 3.3 V and an over-current detection-reset circuit. As mentioned below, the over-current will occur in the case of an SEL. In such a situation, the best way to recover is to perform an immediate hardware reset. Because of the over-current detection and automatic reset function, the processing unit is free from the breakdown caused by the SEL. The circuit measures the current on the high side using a shunt after a common mode filter and regulates 3.3 V from 5 V using a DC/DC converter. (Fig. 7) The voltage drop at the shunt is amplified and compared with the reference voltage using a hysteresis comparator. Then, the polarity is reversed, converting the impedance, and the signal drives the gate of the field-effect transistor (FET) (internal DC/DC). The series resistor and parallel capacitor are put into a gate, and the transient current starts slowly for about 100 ms. The MCP9800, which is a temperature sensor, monitors the board temperature to ensure its ongoing health.

3.4 FPGA Internal Logic design

The internal design of the FPGA was performed using Xilinx Platform Studio. Base System Builder (BSB) was used and the PPC405, processor local bus (PLB), multi port memory controller (MPMC), and XPS interrupt controller (XPS Intc) were made. Furthermore, the IP core that is offered by Xilinx, such as timer, serial parallel interface (SPI), general purpose IO (GPIO), and IIC, was used. The image sensor frame buffer (IMSFB) IP core of insourcing is mentioned later.
The required clock was made using digital clock manager (DCM). 100 MHz is put into DCM1 from a crystal oscillator, and a 100 MHz PLB clock, 200 MHz for MPMC, and 100 MHz of differential clock for DDR2 are made. The 200 MHz output of DCM1 is put into DCM2, and is doubled for PPC405. Because the PLB and PPC405 clock must have the same phase, the source clock must be the same, and the PPC405 clock must be an integral multiple of the PLB clock. The PLB clock must also simultaneously be an integral multiple of the DDR2 clock. Furthermore, since the DCM has many restrictions, the method used to generate in excess of 350 MHz requires an input having more than 175 MHz into the DCM, and it must be doubled using the delay lock loop (DLL). Another clock source, such as an Ethernet MAC and UART IP, serves as an external oscillator.
The reset system has a self-reset from GPIO and the reset from the PIC. When the temperature exceeds 80 degrees, the PIC begins to reset. The PIC is connected to the FPGA by the UART, and the PIC is a function of the acquired temperature, WDT, and configuration change. In many cases, the design

will be simplified if the final PIC is selected from the viewpoint of radiation or heat, rather than the FPGA.

Table 2: The Probability of Anomalies Caused by Irradiation Effect

	Rate in Radiation Test event/minites	Expected Rate in Orbit event/day	Autonomous Reset event/minites
Wihout Watchdog Timer	0.375	1.250	–
With Internal Watchdogof FPGA	0.350	1.167	0.200
With External Watchdog of PIC	0.000	0.000	0.429

4. VERIFICATION ON RADIATION TOLERANCE

To verify the effectiveness and radiation tolerance of the hierarchical monitoring system, verification tests were performed by proton irradiation.

The proton irradiation test was performed at the National Institute of Radiological Sciences (NIRS). The proton beam was formed and energized by the synchrotron, and the energized level was 40 MeV. The beam rate was 4*105 count/cm2/s, which corresponds to a factor of 160 thousands orders of magnitude higher, i.e., a number of 3 year proton is irradiated in ten minute.

Table 2 summarizes the probability of the occurrence of anomalies caused by the irradiation effect. Since the anomalies caused by single event latch up was not observed in this condition, the table only list up the anomalies caused by the single event upset. On average, the probabilities are located at a higher level comparing low performance processors, because the density of the logical element is quite high in Virtex4FX. Even though the anomalies cannot autonomously recovered in the case of internal watchdog timer support, adding external watchdog timer covers the anomalies perfectly, and all anomalies successfully mitigated by using external watchdog timer. The results show that the hierarchical monitoring system is effective for the mitigation of single-event anomalies.

5. CONCLUSION

In this paper, we introduced the outline of the high-performance image acquisition and processing unit for earth observation (HP-IMAP-EO). HP-IMAP-EO was developed utilizing COTS technologies to realize high performance in small-sized satellites. To achieve high reliability against radiation effects, an autonomous hierarchical monitoring system was introduced, and based on verification experiments, the monitoring system was found to be effective in achieving high reliability and survivability. The concept of utilizing the hierarchical monitoring system was considered to be effective not only for image processing systems but also for other on-board equipment to achieve high reliability when utilizing COTS technologies.

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