Increasing IP Reuse Ability by Using OCP-AHB Wrapper for SOC Integration

G.Ramachandra kumar¹, Abdul Rahim²

¹ M.Tech, Scholar at Aurora's Technological & Research Institute (ATRI), Parvathapur, Hyderabad, A.P., India
² Associate professor in department of ECE at Aurora Research & Technological Institute, Parvathapur, Hyderabad, A.P., India

Abstract: As the design of SoC is getting more and more complicated as the IPs (Intellectual Property) reuse ability increasing is the key issue to improve the time of the embedded systems development and integration as the different SoC design environment will affect the IPs reuse ability such as in different system bus and in this paper we implement a standard OCP-AHB bus wrapper which uses the IP with OCP interface that is capable to connect with AMBA 2.0 AHB bus quickly and the IP designer can focus on the development of IP functionalities without considering the data transaction in different interconnects which reduces the IPs development time and increase the reuse ability where the system integration and verification can be accelerated by using the built-in ICE architecture to make the SoC verification more flexible and quickly.

Keywords: SOC, IP, Embedded systems.

1. INTRODUCTION

Now a days the SoC is widely used in the personal electronic products such as Smartphone or tablet PC how to improve the time of the integration and verification of SoC that is becoming an important issue and the key point of the acceleration of the SoC integration and verification is mainly based on how to increase the reuse ability of IPs as the IPs designers need to modify their IPs interface to conform with different system buses and which will affect the IPs reuse ability and costs additional time to re-verify the correctness of the IPs.

As the result in this proposed paper we have implemented the OCP-AHB wrapper with the standard protocol defined by OCP-IP organization [1] where the IP designer just needs to modify the IP’s interface to conform to the OCP standard protocol and then the IP can quickly connect to AMBA 2.0 AHB bus by our OCP-AHB wrapper which will improve the IP reuse ability and the acceleration of the SoC integration.

Furthermore we also added the built-in ICE circuit in our OCP-AHB wrapper that makes the verification process of the SoC more quickly and flexible.

2. RELATED WORK

In the past years the wrapper is designed in two different ways that is one is by automated synthesis such as [3] [4] [5] in [3] is proposed an algorithm which used two different protocol’s FSM to synthesis the corresponding wrapper and in [4] proposes the algorithm for the automated synthesis that can Support non-blocking and out of order mechanism and in [5] the author categorized the interface protocols into 3 groups.

The clock frequency and data width uses the individual group's algorithm to synthesize the corresponding wrapper where the other way is manual design whereas according to the different system buses to design the corresponding bus interface and add some architecture is used to optimize the wrapper performance such as [6] ~ [9] and our OCP-AHB wrapper design.

3. WRAPPER WITH BUILT-IN ICE FUNCTIONALITY

In this section we will be introducing the functionality of OCP-AHB wrapper and built-in ICE.

3.1 Functionality of OCP/AHB Wrapper

The below Figure 1 illustrates the block diagram of the OCP-AHB master/salve wrapper in the embedded system where the OCP signals from the IP are converted to the AHB signals by the OCP-AHB wrapper.

![Figure 1 FSM based architecture of OCP-AHB interface](image)

The OCP-AHB wrapper is intended to support the following transaction modes and processing mechanism:

1. Support SRMD (Single Request Multiple Data) transaction mode.
2. Supports data burst and single read/write transaction mode.
3. Supports the split and retry processing mechanism.
4. Supports master/slave IP busy state processing mechanism.
5. Supports four different registers for in/out version design.
6. Supports different data width (32/64bits) conversion.
3.2 Functionality of Built-in ICE
The Built-in ICE is a transaction-based emulator which is compatible with IEEE 1149.1 JTAG Test Access Port specification which can be easily to take the serial JTAG signals such as: TCK, TDI, TDO, TMS, TRST to setup the Break Point Detection module and then hold the target IP to verify the system or only the target IP where the built-in ICE is embedded in the OCP-AHB master wrapper and will use the scan chain to send new request to bus when the target IP was held or send response to the target IP and in the next section that is IV.B we will discuss the Built-in ICE infrastructure and its test strategy.

4. ORGANIZATION OF THE WRAPPER
In this section we will show how the organization of the OCP-AHB master/salve wrapper and the built-in ICE will introduce each module related to them.

4.1 A. OCP-AHB Wrapper Organization
The below Figure 2 shows the OCP-AHB master wrapper organization that is comprises of OCP-AHB MI FSM along with a Address Generator with a Write Buffer and Read Buffer along with two sets of Decoders and a MUX and a RI(register in) along with RO(register out) modules.

The introduction of each module is described as following:
1 OCP-AHB MI FSM : This module is the kernel unit of wrapper which acts as in charge of converting the signals from the OCP interface of master IP to AMBA AHB bus signals and at the same time controls the other module action.
2 Address Generator: Since we have taken the SRMD (Single Request Multiple Data) transaction mode the master IP only needs to send the first address however AHB bus is MRMD (Multiple Request Multiple Data) transaction mode and it needs address f or each transfer as the Address Generator is in charge of generating address of each transfer according to the burst length and the start address.
3 Write Buffer & Read Buffer: Write Buffer is used to the write data from master IP where the purpose is to improve the performance of data burst write transaction and to reduce the latency of waiting where Read Buffer is used to save the read data from the bus and the purpose is the same as Write Buffer where we are intended to use minimal buffer size that achieves the maximum performance that will be discussed in section 5.
4 Decoder & MUX: are used to decide which entries of the Read/Write Buffer’s data are used to save are further controlled by the WB_wr and RB_wr signals of the OCP-AHB MI FSM.
5 RI & RO: are the two modules that are used to adjust the system cycle time that avoids the critical path getting too long than intended.

Figure 2 OCP/AHB master wrapper organization

In the above Figure 3 shows the organization of OCP-AHB -ve wrapper and the composed modules are the same as the OCP-AHB master wrapper besides the FSM -ve is different where the OCP-AHB SI FSM is in charge of converting the signals from the AHB bus to the OCP interface signals of slave IP.

4.2 Organization of the wrapper with Built-in ICE
The built -in ICE are composed of IEEE 1149.1 TAP Test Access Port and BreakPoint Detection module (BP) along with scan chain and WrapperICE controller are shown in Figure 4.

Figure 3 OCP/AHB slave wrapper organization

1 TAP controller: It is the centric control unit where according to the TAP instruction state machine to setup the relation registers.
2 BreakPoint Detection Unit: is used to detect the target

Figure 4 an OCP/AHB Bus Wrapper with Built-in ICE
IP’s Break Point condition that may be conformed or not if it is conformed then it will notify the Wrapper ICE controller to hold the target IP for further debugging step.

3 **Scan Chain:** includes three different kinds of scan chain such as: ScanChain_BT, ScanChain_AsMaster, ScanChain_SData. ScanChain_BT are used to setup the BreakPoint Detection Unit for specific address or data or the read/write request where ScanChain_AsMaster can send a single request as a Master IP and ScanChain_SData can exchange the Data from AHB to simulate the target IP.

4 **WrapperICE Controller:** It is responsible for controlling the handshake mechanism where the block diagram is showed in Figure 5 and in Figure 6 is a FSM of the WrapperICE Controller where the FSM contains the states such as: WrapperICE_Idle, WrapperICE_Monitor, and Wrapper_ICE_configuration where the WrapperICE Controller is started from WrapperICE_IDLE state when the built-in ICE is idle and when the TRSET is asserted then the state will change to WrapperICE_configuration state and starts to set up the Built-in ICE modules such as BP or Scan Chain. When the user has finished setting up the Built-in ICE environment the state will enter into WrapperICE_Monitor state and start to monitor the target IP transaction until the BP condition that is matched and once the TRESET is asserted the switching takes place between the WrapperICE_Monitor state and the WrapperICE_Configuration state for the next debugging.

5. **SIMULATION RESULTS**

The below is the list of results obtained by providing various inputs:

<table>
<thead>
<tr>
<th>Table 1 OCP master inputs when burst_single_req=0</th>
<th>Input names</th>
<th>values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Wr_bar</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>Addr</td>
<td>$random</td>
<td></td>
</tr>
<tr>
<td>Burst_length</td>
<td>12</td>
<td></td>
</tr>
<tr>
<td>Burst_type</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>Burst_single_reg</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>Wdata</td>
<td>$random</td>
<td></td>
</tr>
<tr>
<td>Wdata_valid</td>
<td>1</td>
<td></td>
</tr>
</tbody>
</table>

When the burst_single_reg is given input as 0 with only one address but in output it produces the address for every request by incrementing 4 bytes that is shown in the below wave form it producing address for every request.

<table>
<thead>
<tr>
<th>Table 2 OCP master inputs when burst_single_req=1</th>
<th>Input names</th>
<th>values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Wr_bar</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>Addr</td>
<td>$random</td>
<td></td>
</tr>
<tr>
<td>Burst_length</td>
<td>12</td>
<td></td>
</tr>
<tr>
<td>Burst_type</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>Burst_single_reg</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>Wdata</td>
<td>$random</td>
<td></td>
</tr>
<tr>
<td>Wdata_valid</td>
<td>1</td>
<td></td>
</tr>
</tbody>
</table>

When burst_single_reg=1 then it will produce only one address for the complete transaction.
The OCP supports single request multiple data but AHB does not support single request multiple data whereas it supports multiple request multiple data and in the above figure AHB Master produces multiple address and for write operation \( \text{HWRITE} = 1 \).

When the detected=1 then it performs in testing operation and when the detected=1 then parallel din values will be assigned as per below:

- \( \text{MAddr\_mux} = \text{parallel\_din}[82:51] \)
- \( \text{MBurstLen\_mux} = \text{parallel\_din}[50:47] \)
- \( \text{MCmd\_mux} = \text{parallel\_din}[46:45] \)
- \( \text{MBurstSeq\_mux} = \text{parallel\_din}[44:43] \)
- \( \text{MTagId\_mux} = \text{parallel\_din}[42:39] \)
- \( \text{MDataTagId\_mux} = \text{parallel\_din}[39:36] \)
- \( \text{MData\_mux} = \text{parallel\_din}[35:3] \)
- \( \text{MDataValid\_mux} = \text{parallel\_din}[2] \)
- \( \text{MRespAccept\_mux} = \text{parallel\_din}[1] \)
- \( \text{MBurstSingleReq\_mux} = \text{parallel\_din}[0] \).

When the value of detected =0 it performs normal operation as in the above figure the input data and output data are same for write operation and \( \text{wdata\_valid} = 1 \) at that time along with the burst_length =12 so as the address is incrementing for 12 times when the burst single req =1.
6. CONCLUSION
In the process of increasint the IP reusability is the main key issue for accelerate the SoC integration as in this paper we have implemented an OCP-AHB wrapper that allows the IP with OCP interface can quickly connects to AMBA AHB bus and also increases the reuse ability of IP and furthermore we add the built-in ICE to make the SoC verification more quickly and flexible.

REFERENCES

AUTHOR
G.RAMACHANDRA KUMAR has completed his B.tech degree in Electronics & Telecommunication Eng from AMIETE in 2011 from Delhi University, Delhi, India and presently he is pursuing his M.Tech degree in VLSI-SD at Aurora’s Technological and Research Institute, Parvathapur, Uppal, Andhra Pradesh, India.

ABDUL RAHIM received his M.Tech degree in Electronics and Communication Engineering from JNTUH, Andhra Pradesh, India. Currently he is working as Associate Professor in Electronics and Communication Engineering department at Aurora’s Technological and Research Institute (ATRI).