Recent Advances in NM-OSCILLATOR Design with CMOS Technology: An Overview

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Abstract: “In Today’s world oscillator is an integrated part of many electronics system”. Application starts from clock generation in microprocessor to carry synthesis in cellular telephones, requiring vastly different oscillator topologies and performance parameter. There are various methods of design of an oscillator like Differential cross coupled, voltage controlled oscillator, single inverter oscillator, Ring oscillator. But within all that the important part is LC Tank circuit. In many topologies the LC Tank circuit used to complete the Barkhausen criteria. The LC Tank circuit attenuates the harmonic of the input current and decides the operating frequency. Also along with that the emphasis is on the techno-logical roadmap in CMOS Design.

Keywords: CMOS, Fundamental oscillator, Design methodology, Phase Noise.

1. Introduction:
A key circuit in modern digital electronics is fundamental oscillator whose output is an AC waveform whose frequency is depends upon the requirement of the application. Fig. 1 shows the operating frequency range of various consumer electronics goods. That shows the frequency range for all these applications are starts from 1 GHz to 4 GHz. Many times on chip oscillator are preferred on the application for which they are using. Similarly they are also preferred with the required Die size, No of component required, Frequency & Amplitude stability, and power consumption.

In RF application the lower phase noise circuits are preferred. Especially cross-coupled LC oscillator is used because of lower phase noise. The phase noise is controlled by making the circuit layout symmetrical & by increasing the Quality factor (Q) of Tank circuit.

When the circuit is initially energized, the only signal in the circuit is Noise. That component of noise, the frequency of which satisfies the phase condition for oscillator, is propagated around the loop with increasing Amplitude. The wider the Tunneling range more difficult to maintain a high stability. Achieving stability is more difficult because the load reactance is affected by Stray capacitance and inductance. Also, because of selectivity of LC circuit, LC oscillator in general does not require amplitude stabilization circuit. Our approach is to find the phenomena’s that arises during the optimization process of CMOS analog component for mili-meter to nano-meter. For any design power consumption of any component & circuit should be minimize or if total minimization is not possible we must keep it low by introduction low power consumption factor that must be minimized. This power consumption factor may be the additional gate tunneling leakage component, complicated design, EMC, EM Interferences.

The rest of the paper is organized as follows. Development in CMOS design technology is explained in section II. NM-Wave oscillator design challenges in section III. Oscillator specification in section IV. Concluding remarks are given in section V.

2. DEVELOPMENT IN CMOS DESIGN TECHNOLOGY:
In the present age the requirement of human being from the machine are increased drastically. Human being take help of applications starts from cellular phone to specific embedded system. In this modern digital age the integrated circuits require more functions within a given silicon area, with reduces fabrication cost, increasing operating frequency & with low power dissipation. In the past SiGe, Inp or GaAs were used for mm-wave circuits. Silicon Germanium (SiGe) is a Si-based compound semiconductor technology offering higher speed transistors than conventional Si devices but with similar cost advantages. The silicon wafer diameters are larger (typically 8” or 12” compared with 4” or 6” for GaAs) and the wafer costs are lower, contributing to a less expensive IC.

But as gallium arsenide (GaAs), provides two fundamental advantages over Silicon, devices (transistor) speed and a semi-insulating substrate. Both factors help with the design of high frequency circuit functions.

Then we have Gallium Nitride (GaN) is also an option for MMICs. Because GaN transistors can operate at much higher temperatures and work at much higher voltages.
than GaAs transistors, they make ideal power amplifiers at microwave frequencies.

Along with that Indium Phosphide (InP), have been shown to offer superior performance to GaAs in terms of gain, higher cutoff frequency, and low noise. However manufacturing expensive due to smaller wafer sizes and increased material fragility.

For the past few years we had introduced to nano meter technology for industrial production of high performance of Integrated circuit. The CMOS technology improvement continues to be driven by the need to integrated more function s within a silicon area.

The phase “Metal Oxide Semiconductor” is a reference to the physical structure of certain field effect transistor, having a metal gate electrode placed on the top of the oxide insulator, which in turns on top of a semiconductor material. These semiconductor materials are polysilicon, also other metal gates are used. Which has high-K dielectric material in the CMOS process, provide by the IBM & Intel for 45 nm technology and beyond. Switching to a new technology node the focus is on the design methodologies, & requires improve technology modes and tools to accurately predict the performance of circuit.

A. General Trends –
Referring to Moore’s law, there is massive improvement in MOS device performances. At ground level; the transistor size, the channel length of MOS devices is automatically sc

The oxide thickness toX is reduced to 1.2 nm (5 atoms). Unfortunately, the gate oxide leakage is exponentially increased, which increases the static power consumption. Reduced tox are known as “metal gates” & based on Nickel-Silicide (NiSi) or Titanium-Nitride (TiN), as illustrated in Fig. 2 below.

Increasing the carrier mobility μ. starting with the 90 nm technology. The carrier mobility is achieved by exploiting the concept of straining electron, which boosts both the n-channel and p-channel transistor performances. It is challengeable task to adopt the technology changes & the consequent changes in design concept & methodology.

B. Present Design Scenario -
The trend of CMOS technology improvement continues to be driven by the need to integrate more Functions within a given silicon area, reduce the fabrication cost, increase operating speed and dissipate less power. Past few years have seen the introduction of nanoscale technologies for industrial production of high performance integrated circuits (IC). Table 1: gives an overview of the key parameters for technological nodes from 130 nm, introduced in 2001, down to 11 nm, which is supposed to be in production in the 2015-2018 timeframe. Mass market manufacturing with the 32 nm technology will be scheduled for 2012.

<table>
<thead>
<tr>
<th>Technology node</th>
<th>130 nm</th>
<th>90 nm</th>
<th>65 nm</th>
<th>45 nm</th>
<th>32 nm</th>
<th>22 nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>First production</td>
<td>2003</td>
<td>2003</td>
<td>2005</td>
<td>2007</td>
<td>2009</td>
<td>2011</td>
</tr>
<tr>
<td>Effective gate length</td>
<td>70 nm</td>
<td>50 nm</td>
<td>35 nm</td>
<td>25 nm</td>
<td>17 nm</td>
<td>12 nm</td>
</tr>
<tr>
<td>Gate material</td>
<td>Poly</td>
<td>Poly</td>
<td>Poly</td>
<td>Metal</td>
<td>Metal</td>
<td>Metal</td>
</tr>
<tr>
<td>Gate dielectric</td>
<td>SiO2</td>
<td>SiO2</td>
<td>SiON</td>
<td>High K</td>
<td>High K</td>
<td>High K</td>
</tr>
<tr>
<td>Kappa (nm²/cV²s)</td>
<td>2.40</td>
<td>1.30</td>
<td>0.60</td>
<td>0.30</td>
<td>0.15</td>
<td>0.08</td>
</tr>
</tbody>
</table>

In early 2007, Intel announced the deployment of hafnium-based high-k dielectrics in conjunction with a metallic gate for components built on 45 nanometer technologies, and has shipped it in the 2007 processor series codenamed Penryn. At the same time, IBM announced plans to transition to high-k materials, also hafnium-based, for some products in 2008. While not identified, it is most likely the dielectrics used by these companies are some form of nitride hafnium silicates (HfSiON), HfO2 and HfSiO are susceptible to crystallization during dopant activation annealing. NEC Electronics has also announced the use of a HfSiON dielectric in their 55 nm Ultimate Low Power technology.
However, even HiSiON is susceptible to trap-related leakage currents, which tend to increase with stress over device lifetime. The higher the hafnium concentration, the more severe the issue. However, there is no guarantee that hafnium will be the future of high-k dielectrics.

The 2006 ITRS (International Technology Roadmap for Semiconductors) roadmap predicted the implementation of high-k materials to be common place in the industry by 2010. Following are the process integration difficult challenges are Scaling si-CMOS, Implementation of high mobility CMOS channel material, scaling of SRAM & DRAM. Reliability due to material, process and structural changes, along with implementation of advanced multi-gate structure, power scaling, Integration of functional diversification. Above challenges are for the analog design industry. [4]- [10]

3. NM-WAVE OSCILLATORS DESIGN CHALLENGES:

In the previous decade, mm-wave circuits were mainly realized using SiGe, InP or GaAs technology. Now, thanks to high-K dielectric material in the CMOS manufacturing technology that of number of component on the die size is increased and the devices are capable of working in the GHz range. Also the speed of MOS transistors has entered the nm-wave region.[7] Now days the CMOS technology is more promising since high integration density and low production cost (At least for high volumes) make the design of nm-wave circuit. On the other hand, it is a challenging task to work with the devices in the 10-60 GHz range because of very high and large frequency span. Today, thanks to technology scaling, nm-wave circuits can be designed in CMOS. But as we are moving towards the UHF, SHF ranges the CMOS technologies works with the very low supply voltages and that is the major design challenge for low phase-noise oscillators. [4] There are various issues when works with the GHz frequencies, to overcome that most of the times enhanced LC tank using bondwire Inductor are proposed. But if we work in the range of 10-60 GHz, those techniques become difficult and the real design challenges arise:

The first challenge is because of the high operating frequency, the high operating frequency is close to the transistor intrinsic frequency Ft. That limits the availability of the power gain at that operating frequency for the transistor.

The second challenge is about the Tuning ratio and the Quality factor (Q). [4] Both these parameter are important for the varactor, because comparing with Q in GHz range, the varactor Q at mm-wave frequencies is lower than the inductor Q that condition dominates the tank circuit quality factor. That is very difficult condition for varactor and layout design for the oscillator performance. [7]

The third challenge is to achieve the good tuning the range, for that the maximum and minimum values of the tank capacitor and inductor should meet a certain ration $\gamma$

$$\gamma = \frac{C_{v_{\text{max}}} - C_{p}}{C_{v_{\text{min}}} + C_{p}} = \frac{1 + \alpha + \beta}{1 + \alpha - \beta}$$

Where, $C_{v}$ is the varactor capacitance and $C_{p}$ is the parasitic capacitor, that includes the capacitance form transistor in cross-coupled pair and buffer stage inductor and interconnect line where the parasitic capacitance is parallel with the varactor capacitance($C_{v_{\text{max}}} \leq C_{p} \leq C_{v_{\text{max}}}$). Where as parameter $\alpha$ and $\beta$ are representing the varactor tuning ratio and the ration of parasitic to varactor capacitance resp. From equation $\gamma$ the tuning range can be increased either by increasing $\alpha$ or by decreasing $\beta$, by reducing the capacitive loading from buffer stage or by increasing the varactor value $\beta$ can be reduced. But by reduction of capacitive loading that results in the less output power. To increase the output power, an additional output power stage is should be added but that results in the unwanted DC power consumption. Similarly by increasing varactor value $\alpha$ can be increases that decreases the tank impedance, to avoid that condition transistor with large Negative resistance will be needed, otherwise the oscillations will not be started. Also increasing the varactor value will deteriorate the tank quality factor Q-tank, thus that causes the increase of the phase noise according to the lessons formula. [7]

The fourth challenge is to keep the very large oscillator gain (Kvco) and the worst reactive linearity. The large Kvco is caused by a tuning range in a low supply voltage, non-linear transistor capacitance like Cgs, Cds becomes a large portion of the tank capacitance, thus deteriorating the tank reactive linearity further. For example, if only considering the Kvco effect, a series resistance of 10 ohm at the tuning-voltage node will generate a phase noise of -116.9 dBc/Hz @ 1 MHz offset.

If the tail current MOS is used in oscillator, it contributes three noise the tank loss, the noise of cross coupled pair and the noise of tail current. Generally phase noise is because of direct phase noise generation i.e. physical interpretation of lesson’s noise factor F, and due to tank indirect nonlinear AM-PM conversion process considered.
when the phase is generated as the time integration of frequency. [2] To achieve the good phase noise by reducing the effect of noise contribution of various component of oscillator with the high tank Q also increase the amplitude across the tank. Most of the times varactor are NMOS transistor in inversion mode. The varactor is a crucial component in mm wave circuit design and fig. 4 shows the important loss sources and parasitic capacitances in capacitor. The channel resistance $R_{ch}$, interconnection loss like gate resistance $R_{poly}$ greatly affects the Q. The phase noise is also affected by the varactor control line, the power supply and the tank. We cannot achieve the good phase noise with increasing the tank Q factor, we need to take care of the low supply disturbances, an amplifies with high linearity should be used. The quality factor can be increased by reducing the gate length and width, but this will increases the fringing capacitance $C_{par}$ which will consequently reduces the tuning ratio. [4]

Sometimes the inductive division technique has the following three advantages: first, it will increase the signal amplitude across the varactor and to a certain degree improve the tank reactive power balance, resulting in a better phase noise; second, it realizes the isolation between varactors and parasitic capacitance generated from transistors and interconnect lines, thereby improving the tuning range; third it helps to achieve a very compact layout with good decoupling to supply voltage.

In the deep submicron technology the gate resistance $R_{g0}$ provides the great challenge to design high-frequency oscillator design. The fig. 5 shows the three components that contribute to the gate resistance contact. That fact arise because of the following effects the poly-metal contact resistance $R_{cont}$ (contributes about $15 \Omega$ per contact), the distributed resistance $R_{dist}$ and the extrinsic resistance $R_{ex}$ with a sheet resistance of about $10 \Omega$/square and the required spacing between the contact and the channel, $R_{c0} = 35 \Omega$ (for $L=60 \text{ nm}$) and the contact (for nM). It is desirable to contact the gate on both ends to reduce $R_{dist}$ by a factor of 4, and minimize the width so that $R_{dist}/3$ is well below the unscalable component, $R_{cont} = R_{ex}$. However, very narrow gates exhibit a longer equivalent channel length due to the distribution of dopants toward the shallow trench surrounding the transistor. As a compromise, in this work each gate finger has W/L of $0.4 \mu m/60 \text{ nm}$ and contacts on both ends, yielding an equivalent lumped resistance of $30 \Omega$. [3]

While design of the nM oscillator we should care of the noise sources that are cyclostationary because of the periodic changes in current and voltage of the active devices.

A. Stationary Noise sources:- In the stationary noise approach the power density of the noise sources are evaluated at the most selective time(i.e., the zero crossing of the differential tank voltage) to estimate the effect of these sources.

$$\frac{\Delta f}{f_0} = 4kT\mu Cox \frac{W}{L} \left(V_{gs} - V_T\right)$$

(2)

Where $\mu$ is the mobility of the carriers in the channel, Cox is the oxide capacitance per unit area, W and L are the width and length of the MOS transistor, respectively, $V_{gs}$ is the gate source voltage, and $V_T$ is the threshold voltage. This equation is valid for both short- and long-channel regimes of operation. In addition to these sources, the contribution of the effective series resistance of the inductor $r_i$, caused by ohmic losses in the metal and substrate is given by,

$$\frac{\Delta f}{f_0} = 4kT\mu Cox \frac{W}{L} \left(V_{gs} - V_T\right)$$

(3)

Where, $R_p \approx Q^2/2 = (Lw)^2/2\Omega$ is the equivalent parallel resistance at the frequency of oscillation. [6]

B. Tail current noise sources: - If the differential transistor is used in the design of the oscillator then the current through the differential oscillator is equal to the tail current.

However, this assumption can break down if there is a capacitor in parallel with the tail current source. This capacitor provides an alternative path for the tail current. If the tail capacitor is large, the differential pair transistors might carry very little current for a fraction of the cycle.[6] To investigate further the effect of this capacitor, the simulation LC oscillator was repeated with a 10-pF was repeated with a 10-pF. The use of an extra tail capacitor can improve the phase-noise behavior of the differential LC oscillator.
The tail capacitor attenuates the voltage variations on the tail node and therefore reduces the channel length modulation of the tail-current source. This effect results in more symmetric waveforms and smaller harmonic distortion in the output of the oscillator. One disadvantage of such a tail capacitor is that it reduces the output impedance of the tail-current source at high frequencies. This reduction increases the sensitivity of the oscillator to supply-voltage variations. The effect of tail current and equivalent tank loading on voltage amplitude.

[6]

4. Oscillator Specification:

The important thing is to achieve the 360° phase shift at the output. That is achieved by providing the two identical cascade sections to the oscillator whose outputs are 180° out of phase. But doing that is very difficult to keep the oscillator amplitude, average supply current within the required limit. Also two major noises appear that are at high frequency the channel thermal noise and at the low frequency flicker noise. [9] Following are the specification that we should take care of,

A. Output Voltage amplitude - Generally the MOS used are the combination of the PMOS & NMOS pair and the NMOS are faster than the PMOS transistor because of the different mobility and threshold voltage. But that speed discrepancy can be avoided by the careful selection of the width ratio of the two transistors. By proper sizing of the transistor, we can conclude dc level of drain voltage in two stages are the same and equal to Vdd/2. But the main problem is one of the movement in the operation will come in which both the transistor will be in the Non linear region of their operation and output current has no even harmonics including the DC component.

B. Power consumption - To define the power consumption of the oscillator first of all the need is to define the overall performance of the single stage CMOS oscillator. In order to have the quantitative estimation of the oscillator power consumption, we should be able to obtain the analytic relation for the DC current drawn from supply by each oscillator stage.[8]

C. Phase Noise - The most sensitive time for the transistors channel thermal noise sources is when the zero crossing of the differential tank voltage occurs. The phase noise is very important for the starting of the oscillation but is very important to maintain that also.[8] Following are the methods to improve the noise. The first one is A high Q-factor inductor: - In LC oscillators, the resonator acts as a bandpass filter to reject undesired noise components. If a higher Q-factor inductor is applied in the tank, a narrower “shock” around the carrier can be expected, which results in a better phase noise. Since all the noise components are folded around he carrier they will be suppressed by a higher Q-factor resonator, this method is most efficient compared with other phase noise improvement methods. In the meanwhile, a higher Q-factor inductor indicates a smaller in-band noise of the tank, which leads to a lower phase noise.[5] The second one is the Increase the core current: - Normally, phase noise is characterized by the ratio of phase noise power compared to the signal power. In General, larger signal can be achieved by increasing the core current at the cost of larger power consumption. The output voltage swing of LC oscillator is limited by the saturation conditions of the cross-coupled transistors. When this saturation condition is met, a further increase of the core current will have no effect. For this reason, also the saturation condition of the transistor core needs to be optimized. [2] The third one is the LC Filtering Technique: - To reduce the contribution of second harmonic noise in the tail current source to the phase noise of the oscillator, a filtering technique can be applied. As shown in Fig. 7 below, a large capacitor is placed in parallel with the tail current source to short noise frequencies around0 to 20. To raise the impedance, an inductor is inserted between the tail current source and common mode point of the switching transistor pair.

![Fig. 7 Tail-biased Oscillator with noise filter](image)

And the fourth one is increasing the area of cross-coupled transistor: - The noise due to the base resistance of cross-coupled transistors is converted into phase noise by the spectrum folding mechanism described by Samori’s nonlinear phase model. If the area of cross-coupled transistors is increased, the base resistance is reduced, consequently, yielding a smaller voltage noise source and correspondingly a lower phase noise. [5]

5. CONCLUSION:

This review note has illustrated the trends in CMOS technology and introduced the 45-nm technology generation, based on technology information available from integrate circuit manufacturers. A set of specific topics has been addressed, including the new gate dielectric, gate stack and the strained silicon technique for enhanced mobility & roadmap of available technology to design the integrated circuits. Along with the nM wave oscillator design challenges that
use the high K-dielectric material that avoids the use of InP or GaAs technology. With the use of that device scaling is possible, the devices are more fast and compatible to our advanced requirements, and power consumption is reduced.

Also the most important factor in oscillator design to improve the phase noise. Also the challenges about high operating frequency, achieve good tuning range, Quality factor and large oscillator gain. The noise sources at SHF frequency range stationary and tail current noise. To achieve good phase noise, special attention should be paid to the quality factor of the tank and the harmonic level of the oscillator output signal. To reduce the harmonic levels, a pseudo-differential cross-coupled pair is used instead of a tail-current biased differential pair. These assumptions are very helpful to design the SHF devices.

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