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Comparative Performance Analysis of a High Speed 2-D Discrete Wavelet Transform Using Three Different Architectures

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Abstract: ***The discrete wavelet transform is used extensively in many applications, such as computer vision, pattern recognition, sub band coding, speech analysis etc. because of its capability of decomposing a signal at multiple resolution levels. It is also used in the field of image processing for texture discrimination, fractal analysis, and image compression. This 2-D DWT requires massive computations and hence there is a need for use of efficient architectures for the implementation of 2-D DWT. This paper focuses on comparing the performance of three types of architectures that is intended to compute the discrete wavelet transform of a 2-D signal at a faster rate. Here we present a comparative study of the computation time for a high speed 2-D discrete wavelet transform implementation using three different architectures: single-processor architecture, parallel-processor architecture and pipeline architecture.***

Keywords: Discrete wavelet transform, discrete cosine transform, fractal analysis, texture discrimination.

1. INTRODUCTION

During last few years a great amount of attention has been given to signal processing applications. These applications include multi-resolution signal processing, computer vision, sub band coding, speech, image and video compression, image recognition system and so on. Usually the discrete cosine transform is used for realizing signal compression. However, DCT is confined to poor subjective and objective image quality at high compression rate to the negative effects of blackness. The discrete wavelet transform is a mathematical technique that provides a new method for signal processing. The DWT decomposes a signal in the time domain by using dilated / contracted and translated versions of a single basis function, named the prototype wavelet. The DWT decomposes data into several components of different frequencies, such that we can have arbitrarily good time resolution at high frequencies and arbitrarily good frequency resolution at low frequencies. In case of image coding, the DWT has an advantage over other transforms in performing a multi-resolution analysis of image. The basis functions of DWT match the human visual profiles resulting in high compression ratios with subjectively pleasing images at low bit rates. In the field of image processing, the two-dimensional DWT has been recently used as a powerful tool for texture discrimination, fractal analysis, and image compression. Nevertheless, 2-D DWT demands massive computations. As a consequence, in applications requiring real-time performances such as on-line video and image coding, the use of either parallel implementations or efficient VLSI application-specific integrated circuits is strategic. Therefore, a large number of VLSI architectures have been realized or proposed that implement the 2-D DWT.

2. 2-D DISCRETE WAVELET TRANSFORM

Wavelet transform can be seen as a decomposition of the signal $f(x)$ into a number of resolution levels with $j = 1, 2, 3, \cdots$. In order to decompose a 2-D signal, the 1-D scaling and wavelet functions have to be extended to two dimensions. A 2-D function can be obtained simply by multiplying two 1-D functions along x and y directions, respectively. Thus, the 2-D scaling function can be generated from the 1-D scaling functions, as

$$\Phi(x, y) = \Phi(x)\,\Phi(y) \quad (1)$$

The 2-D scaling coefficients associated with the scale index j for the 2-D DWT can be obtained as

$$c(j, k_x, k_y) = \sum_{mx}\sum_{my} h(m_y - 2k_y)\, h(m_x - 2k_x)\, c(j+1, m_x, m_y) \quad (2)$$

Three types of 2-D wavelet functions, namely, vertical wavelet $\psi^{(v)}(x)$, horizontal wavelet $\psi^{(h)}(x)$, and diagonal wavelet $\psi^{(d)}(x)$, can be obtained using the 1-D scaling and wavelet functions as

$$\psi^{(v)}(x, y) = \Phi(x)\,\psi(y) \quad (3)$$
$$\psi^{(h)}(x, y) = \psi(x)\,\Phi(y) \quad (4)$$
$$\psi^{(d)}(x, y) = \psi(x)\,\psi(y) \quad (5)$$

This leads to three types of wavelet coefficients given by

$$w^{(v)}(j, k_x, k_y) = \sum_{mx}\sum_{my} g(m_y - 2k_y)\, h(m_x - 2k_x)\, c(j+1, m_x, m_y) \quad (6)$$

$$w^{(h)}(j, k_x, k_y) = \sum_{mx}\sum_{my} h(m_y - 2k_y)\, g(m_x - 2k_x)\, c(j+1, m_x, m_y) \quad (7)$$

$$w^{(d)}(j, k_x, k_y) = \sum_{mx}\sum_{my} g(m_y - 2k_y)\, g(m_x - 2k_x)\, c(j+1, m_x, m_y) \quad (8)$$

It is seen from (2) and (6) to (8) that, the four components of the 2-D DWT at the resolution level with a scale index *j* are produced using the scaling coefficients at the level with a scale index (*j*+1).

2.1 Separable approach for the computation of 2-D DWT

A straightforward way to perform the computation of the 2-D DWT is to use a separable approach. In the separable approach, the impulse response G(z1, z2) of each 2-D filter used for the DWT computation is product separable, i.e., G(z1, z2) = G1(z1)G2(z2), The filter G1(z1) is used to process the 2-D data of successive rows (columns). Then, the resulting 2-D data is processed successively along the columns (rows) using the filter G2(z2). A binary tree representation for a 2-level DWT computation of 2-D signal s(n1, n2) based on the separable approach is shown in Figure 1.

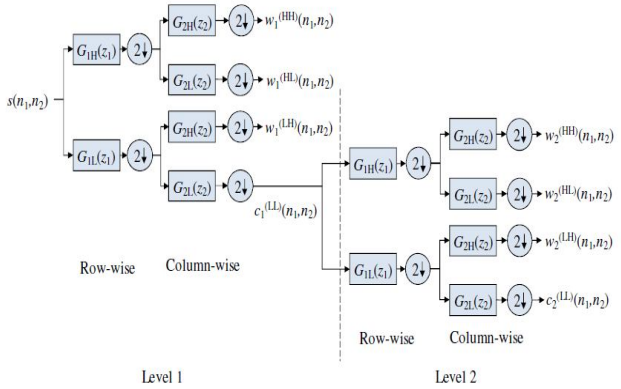

Figure 1 Binary tree representation of the computation of a 2-level 2-D DWT based on separable approach

It is seen from this figure that the computation for the decomposition of a given level j consists of two decomposition steps: row-wise decomposition of the 2-D input data and column-wise decomposition of the 2-D data resulting from the row-wise decomposition. In the row-wise decomposition, each row of the 2-D input data is filtered using the two-channel horizontal filter bank (G1H(z1) or G1L(z1)) and then down sampled by a factor of two, to produce horizontal high pass and low pass components, each component having one-half of the numbers of samples in the rows of the 2-D input data. In the column-wise decomposition, each column of the two resulting components is filtered by using the two-channel vertical filter bank (G2H(z2) or G2L(z2)) and down sampled by a factor of two so that in total four components, specified as the HH component wj (HH)(n1, n2), LH component wj (LH)(n1, n2), HL component wj (HL)(n1, n2) and LL component cj (LL)(n1, n2), are obtained as outputs of the given level j. Among the four outputs, only the LL component cj (LL)(n1, n2) is used for the computation of the next resolution level, which is an iteration of the above two steps.

2.2 Non-Separable approach for the computation of 2-D DWT

Obviously, separable approach is a simple way to compute the 2-D DWT. However, separable filters being a special class of 2-D filters are not capable to approximate well all the arbitrary frequency responses. In this regard, a non-separable approach of the 2-D computation provides more flexibility. In the non-separable approach depicted in Figure 2, the DWT of a 2-D signal s(n1, n2) is computed by carrying out four separate 2-D filtering operations using four 2-D filters: a high pass-high pass (HH) filter GHH(z1, z2), a high pass-low pass (HL) filter GHL(z1, z2), a low pass-high pass (LH) filter GLH(z1, z2), and a low pass-low pass (LL) filter GLL(z1, z2). The output signals of these four filters are then decimated by a factor of two in the horizontal and vertical directions producing, respectively, the HH, HL, LH and LL components**.**

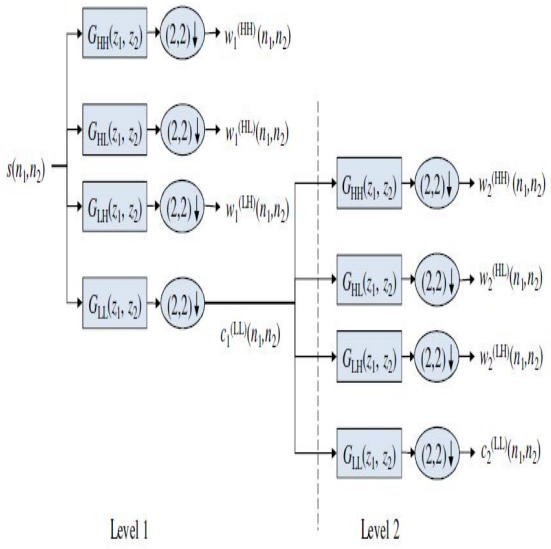

Figure 2 Representation of the computation of a 2-level 2-D DWT based on non-separable approach

3. THREE TYPES OF ARCHITECTURES

In recent years, much architecture has been proposed for the DWT computation. These architectures aim at providing high performances, in terms of their speed, area, throughput, latency and power consumption. The filtering operation involved in the DWT computation is usually the convolution operation, that is, FIR filtering. The structure of the filter could be a direct realization, or it could be a systolic, lattice, bitwise or lifting based realization, depending on the way that the basic convolution operation is manipulated or formulated. The lifting-scheme based filtering operation requires a cascade of lifting steps, and thus, leads to a large latency and a long critical path of the resulting lifting architecture. The filtering operation is carried out by using a processor that employs a certain type of filter structure. The architecture may use one or multiple such processors to perform the DWT computation. For the purpose of reviewing these existing architectures, we categorize them as single-processor architectures, parallel-processor architectures and pipeline architectures, depending on their configuration and the number of processors used by them. In a single-processor architecture, only one processor carries out the filtering

operation by computing the samples of the DWT in a recursive manner. This is illustrated in Figure 3.

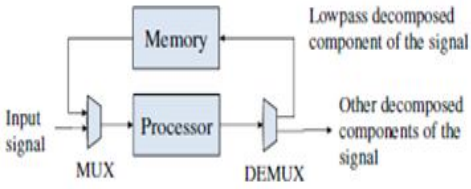

Figure 3 Block diagram of single-processor architecture

In a parallel-processor architecture, multiple processors are used to carry out the filtering operations so that more than one sample is computed at a time. In this type of architecture, the filtering operations to decompose the input signal into various components are carried out in parallel, whereas the computations of various resolution levels are still performed recursively by the parallel processors. Figure 4 shows the block diagram of parallel-processor architecture.In a pipeline architecture, a certain number of stages, each consisting of one or more processors, are pipelined so that the computation of each decomposition level as well as that of the multiple resolution levels are performed in parallel. Figure 5 depicts the block diagram for the pipeline architecture. In each of these three broad categories, architectures may differ considerably because of the internal structures of processors employed for the filtering operation.

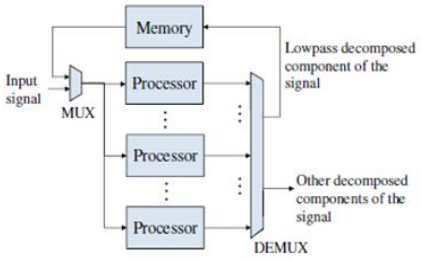

Figure 4 Block diagram of parallel-processor architecture

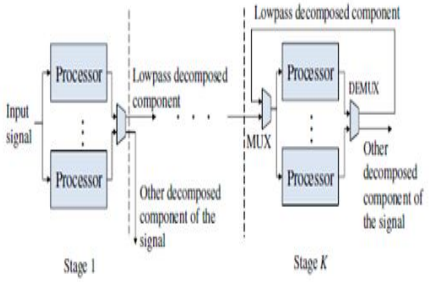

Figure 5 Block diagram of pipeline architecture

4. RESULTS AND ANALYSIS

For the purpose of evaluating the performance of a computational architecture, one needs to make use of certain metrics that characterize the architecture in terms of the hardware resources used and the computation time. The computation time, in general, is technology dependent. However, a metric that is technology independent and can be used to determine the computation time T is the number of clock cycles (N_{CLK}) elapsed between the first and the last samples inputted to the architecture. Assuming that one clock period is T_c, the total computation time can then be obtained as $T=N_{CLK}T_c$.

In order to compare the computation time of the three types of architectures, the clock period for three levels decomposition of an image are given in Table 1. It is seen from this table that the single processor architecture and the parallel processor architecture require, respectively, 24.4ns and 17.8ns, where as the pipeline architecture is found to perform well with a clock period as short as 17.346 ns (i.e. a maximum clock frequency of 57.651 MHz). When compared to single processing and parallel processing architecture the pipeline scheme computes the 2-D DWT of a 2-D signal at a higher speed. This is also illustrated through a graph as shown in Figure 6.

Table 1: Comparison of computation time for three types of architectures

Type of Architecture	T_c in nanoseconds
Single-processor architecture	24.4
Parallel-processor architecture	17.8
Pipeline architecture	17.34

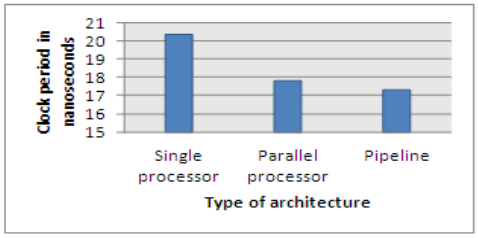

Figure 6 Graph illustrating the computation time for three types of architectures.

5. CONCLUSION

In this paper we presented a comparative study of the computation time for a high speed 2-D discrete wavelet transform implementation using three different architectures: single-processor architecture, parallel-processor architecture and pipeline architecture. It is seen that the single processor architecture requires a clock period of 24.4ns for the three level decomposition of an image. The same task is accomplished with a clock period of 17.8ns by using parallel-processor architecture, where as the pipeline architecture uses a clock period as short as 17.346ns. Hence comparatively the pipeline architecture is preferred to be the best for the implementation of 2-D discrete wavelet transform in real time applications.

References

[1] S.Mallat, "Wavelet for a vision," Proc. of IEEE, vol. 84, on. 4, pp. 604-614, Apr. 1996.
[2] M. Vetterli and J. Kovacevic, Wavelets and subband coding. Englewood Cliffs, NJ: Prentice Hall, 1995.

[3] S. Kadambe and G. F. Boudreaux-Bartels, " Application of the wavelet transform for pitch detection of speech signals, " IEEE Trans. Inform. Theory, vol. 38, no. 2, pp. 917-924, Mar. 1992.
[4] A. S. Lewis and G. Knowles. " Image compression using 2-D wavelet transform," IEEE Trans. Image Process., vol. 1, no. 2, pp. 244-250, Apr. 1992.
[5] M. Antonini, M. Barlaud, P. Mathieu, and I. Daubechies, " Image coding using wavelet transform," IEEE Trans. Image Process., vol. 1, no. 2, pp. 205-220, Apr. 1992.
[6] A. Averbuch, D. Lazar, and M. Israeli, "Image compression using wavelet transform and multi-resolution decomposition," IEEE Trans. Image Process., vol. 5, no. 1, pp. 4-15, Jan.1996.
[7] G. M. Davis, "A wavelet-based analysis of fractal image compression," IEEE Trans. Image Process., vol. 7, no. 2, pp. 141-154, Feb. 1998.
[8] Y. Q. Zhang and S. Zafar, "Motion-compensated wavelet transform coding for color video compression," IEEE Trans. Circuits and Syst. for Viedo Tech., vol. 2, no. 3, pp. 285-296, Sept. 1992.
[9] T. H. Reeves and M. E. Jernigan. "Multe-scale-based image enhancement," in Proc. IEEE Int. Conf. Electrical and Computer Engineering, vol.2, May 1997, pp. 500-503.
[10] D. Marpe and H. L. Cycon, "Very low bit-rate video coding using wavelet-based techniques" IEEE Trans. Circuits and Syst. for Video Tech., vol. 9, no. 1, pp. 85-94, Feb. 1999.
[11] I. Daubechies, "The wavelet transform, time frequency, localization and signal analysis," IEEE Trans. Inform. Theory, vol. 36, pp. 961-1005, Sept. 1990.
[12] I. Daubechies, Ten Lecture on Wavelet. Philadelpha, PA: SIAM, 1992.
[13] S. G. Mallat, "A theory for quadriresolution signal decomposition: The wavelet representation," IEEE Trans. Pattern Ana. Machine Intell., vol. 2, pp. 674-693, 1989.
[14] A.S. Lewis and G. Knowles, "VLSI architecture for 2D Daubechies wavelet transform without multipliers," Electron. Lett., vol. 27, no. 2, pp.171−173, Jan. 1991.
[15] S. Movva, S. Srinivasan, "A novel architecture for lifting-based discrete wavelet transform for JPEG2000 standard suitable for VLSI implementation," in Proc. IEEE 16th Int. Conf. VLSI Design, 4−8 Jan. 2003, pp. 202- 207.
[16] K.C. Hung, Y.S. Hung, and Y.J. Huang, "A nonseparable VLSI architecture for the two-dimensional discrete periodized wavelet transform," IEEE Trans. VLSI Systems, vol. 9, no. 5, pp. 565−576, Oct. 2001.
[17] I. S. Uzun and A. Amira, "Design and FPGA implementation of non-separable 2- D biorthogonal wavelet transforms for image/video coding," in Proc. IEEE Int. Conf. Image Processing (ICIP), 24−27 Oct. 2004, vol.4, pp. 2825−2828.
[18] C. Chakrabarti and C. Mumford, "Efficient realizations of analysis and synthesis filters based on the 2-D discrete wavelet transform," in Proc. IEEE Int. Conf. Audio, Speech, and Signal Processing, May 1996, pp. 3256–3259.
[19] P. Wu and L. Chen, "An efficient architecture for two-dimensional discrete wavelet transform," IEEE Trans. Circuits and Systems for Video Technology, vol. 11, no. 4, pp. 536 545, Apr. 2001.
[20] J. M. Jou, P. Y. Chen, Y. H. Shiau, and M. S. Liang, "A scalable pipelined architecture for separable 2 D discrete wavelet transform," in Proc. the Asia and South Pacific Design Automation Conf. (ASP-DAC), 18−21 Jan. 1999, vol. 1, pp. 205−208.
[21] K. Mihic, "An efficient semi-systolic architecture for 2-D discrete wavelet transform," in Proc. IEEE European Conf. Circuit Theory and Design (ECCTD), Espoo, Finland, 28−31 Aug. 2001, pp. 333−336.
[22] F. Marino, "Efficient high-speed/low-power pipelined architecture for the direct 2-D discrete wavelet transform," IEEE Trans. Circuits and Systems II: Analog and Digital Signal Processing, vol. 47, no. 12, pp. 1476−1491, Dec. 2000.

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