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Design of an Optimized CMOS Thermometric Type Digital to Analog Converter

Neha Gulati[1], Heena Gulati[2]

[1]Global Institutes, Department of Electronics and Communication, Amrisar, Punjab

[2]Global Institutes, Department of Electronics and Communication, Amrisar, Punjab

Abstract

This paper explicates the design of thermometric type of digital to analog converter for the data communication applications which require large accuracy and full scale output voltage evaluated is 1.4 V along with very less power consumption of 2.4mW. Implementation of data converter is achieved with thermometric type of digital to analog converter and layout is realized in 180nm technology. A 4 to 15 decoder is designed which transform the binary to thermometric required for architecture of thermometric current steering digital to analog converter.

Keywords: Current Steering DAC, Thermometric type of DAC, 4:15 Decoder.

1. INTRODUCTION

The digital signal processing bought a large revolutionary change in the world of data communication with the invention of numerous techniques of digital to analog conversion. Digital to analog converter involves the transformation of discrete digitized signal into non-discrete or continuous signal. The data converters are utilized almost in every field of communication. For instance, satellite communication, wireless communication, optical fiber communication and digital communication. These data converters are proved to be advantageous based on the use of different techniques incorporated on the mixed signal circuits or chips. One amongst those techniques is current steering technique of conversion of digital to analog signal. Current steering DAC subsumes greater amount of benefits as compare to other data converters in the terms of power consumption, data conversion speed, linearity of response accuracy, occurrence of glitches and complexity. Current steering type of data converter utilizes the current in the entire process of conversion. At the output, the current is changed into an analog voltage. Current steering data converter is designed with the matched current sources. The resistor is employed at the output section of the architecture which is required for the transformation of current into voltage as illustrated in Fig. 1. There is no necessity of output buffer. This quality of current steering type of data converter is preferable for the design of circuits with fast rate of data conversion with greater accuracy and without parasitic [1]. Current Steering type of digital to analog converter can be designed with two types, Binary Weighted type digital to analog converter and Thermometric type digital to analog converter. The architecture of thermometric type of digital to analog converter is demonstrated in this paper introduction of the paper should explain the nature of the problem, previous work, purpose, and the contribution of the paper. The contents of each section may be provided to understand easily about the paper.

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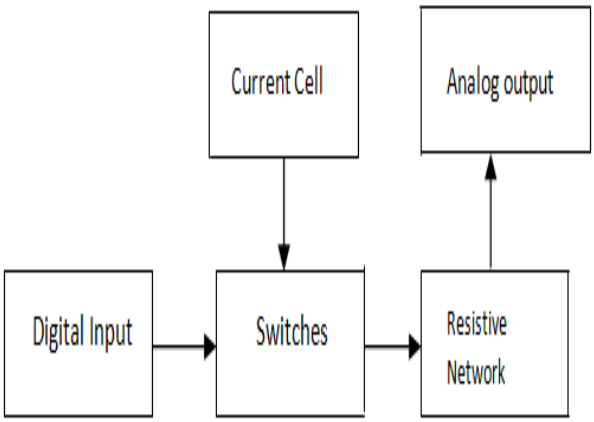

Figure 1 General Block Diagram of Current Steering DAC

Current Steering type of data converter is designed using binary weighted scheme and thermometric scheme has numerous benefits as well as drawbacks. Binary weighted scheme is implemented utilizing weighted current sources attached with the switches. The main limitation of binary weighted scheme is large amount of glitches is obtained in output which emulates to non-linearity [2]. In this paper, thermometric scheme is designed and analyzed using Cadence Virtuoso schematic editor with CMOS 180nm technology and post layout verification is accomplished which comprises of Design Rule Check (DRC) and Layout Versus Schematic utilizing Assura tool.

2. DESCRIPTION OF THE PAPER

The paper explains the implementation of Thermometric type of data converter with reduced glitches and realized using CMOS 180nm technology in cadence virtuoso environment. The maintenance of paper demonstrated in

such a manner that Section 3 presents the general design and schematic diagram of Thermometric type of DAC. Section 4 depicts the designing of decoder which transforms code from binary to thermometer on cadence virtuoso tool. Section 5 gives the description of Binary code transformation to thermometer code. Section 6, 7, 8, 9 enlightens the simulation results and design specifications of DAC.

3. Design of Thermometric type of DAC

The architecture of Thermometric scheme of DAC is designed with 4 to 15 bit binary to thermometer code which transforms the binary code to thermometer code. The output of decoder is driven to each current cell which comprises of current sources and switches with proper aspect ratio. The architecture makes use of differential switches and CMOS current sources. The digital inputs are provided to switches which turn off and on in accordance with input values. The switches upon activation pass or steer the current to the output section of the design. The current is transformed to an analog voltage with the assistance of resistor.

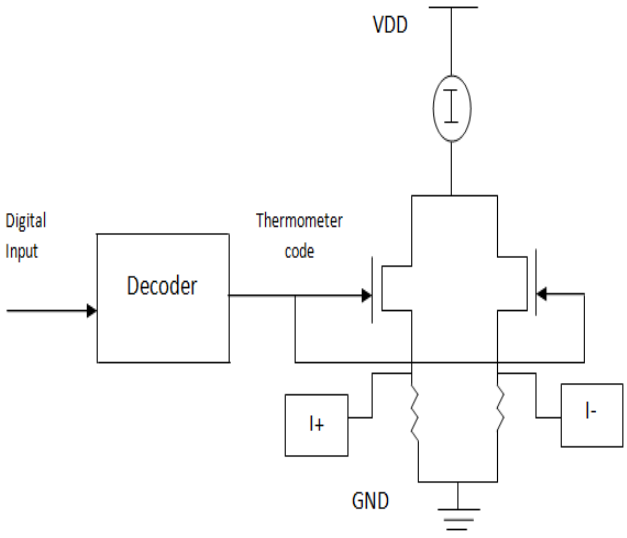

Figure 2 Design of Thermometric type of DAC

Thermometric type of digital to analog converter is suitable for the applications where high accuracy, linearity and monotonicity are required. The architecture of thermometric scheme of digital to analog converter is implemented with the use of 'N' number of current cell for N-bit thermometric type DAC. As illustrated in Fig. 4, four input decoder drives the output to fifteen current cells. Each current cell comprises of current sources and switches which drives the current to the output part of architecture. The schematic design of Thermometric type of DAC is realized using Cadence virtuoso tool and simulations is analyzed with simulation tool.

The Thermometric DAC confirms a good dynamic and static performance. The Dynamic characteristics are affected in high frequencies and Dynamic errors constitute to glitches and parasitic capacitance occurred in wires. The Static characteristics vary in low frequency and Static errors prominent when there is mismatch between current sources and switches [5]. The code is transformed to all zeros to all ones instantly is termed as thermometer code.

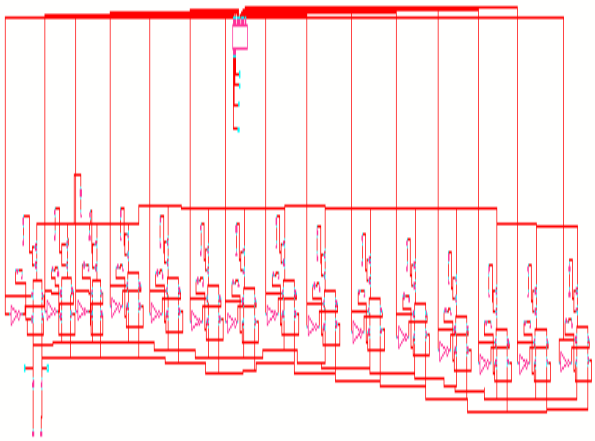

Figure 3 Schematic Design of Thermometer type of DAC

4. Binary to Thermometer Decoder

The general idea of decoder is based upon the fact that the decoder is the component which chooses one of 2^n outputs by decoding the binary value on the 'n' inputs. The binary to thermometer decoder is designed with utilization of gates like AND, OR, NOT gate with CMOS 180nm technology.

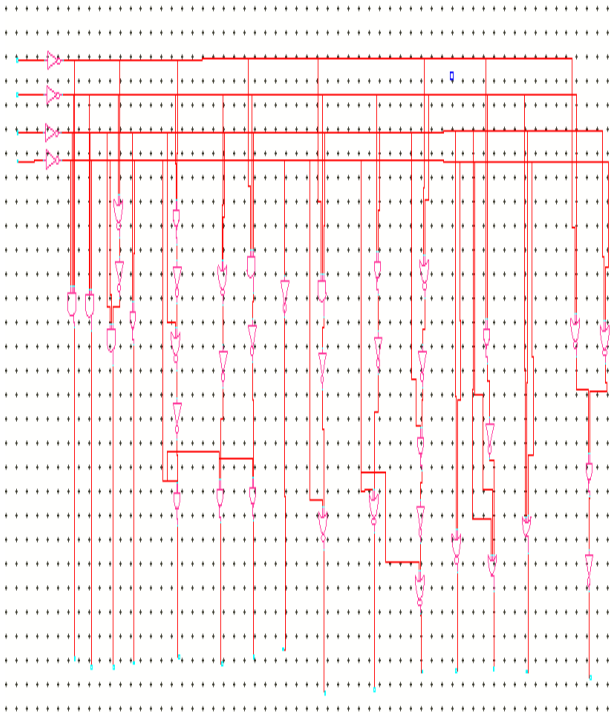

Figure 4 Four to Fifteen Binary to Thermometer Decoder

5.BINARY TO THERMOMETER CODE

The decoder utilized for effective transformation of code from binary to thermometer for the realization of thermometric type digital to analog converter. The proposed design of data converter has been implemented with the assistance of binary to thermometer decoder which selects the particular output by decoding the binary value of input code. The code is assigned to all the current cells through binary to thermometer decoder. Based upon the decoder input which has been provided to current cells, current steering operation is performed utilizing the decoded inputs. The thermometer code ameliorates the linearity by reducing glitches. The non-linearity in thermometer architecture due to errors subsumes Integral non-linearity and Differential non-linearity. The Integral non-linearity is considered for whole slope of output waveform of thermometer design of DAC. The non-linearities are greatly reduced to large extent by employing thermometer code. The monotonicity is therefore also mitigates with thermometer architecture of DAC.

6.SIMULATION RESULTS OF PROPOSED DAC

The simulation result of decoder involves each inputted bit is decoded and is illustrated in Fig. 5 a). Four bits are provided to decoder as input and four bits binary input is changed to sixteen bit of thermometer code which is further given to current cell for the proper functioning of digital to analog converter which confirms linearity.

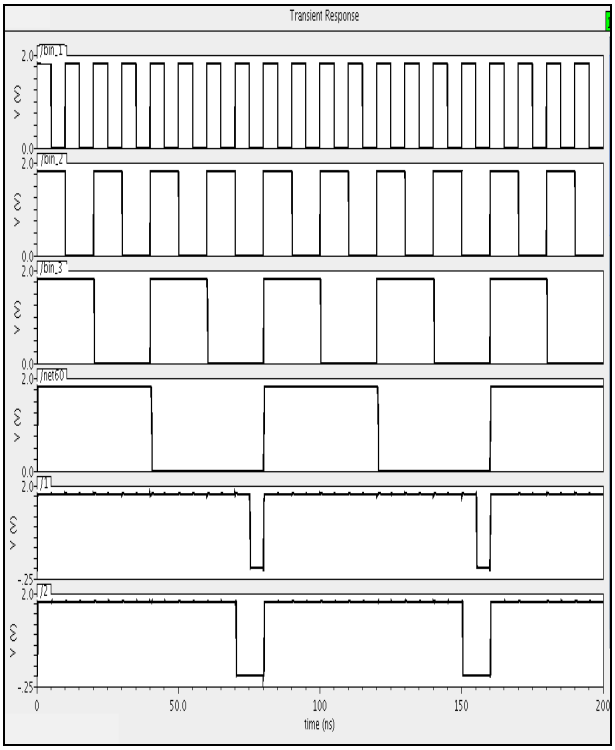

Figure 5 a) Simulation Result of Binary to Thermometer Decoder

The Conversion of binary to thermometer code after applying four binary bits as illustrated in Fig. 5 a) such that first four bits are inputs to decoder and rest are the outputs of decoder which are shown in Fig. 5 b) and Fig. 5 c) subsequently.

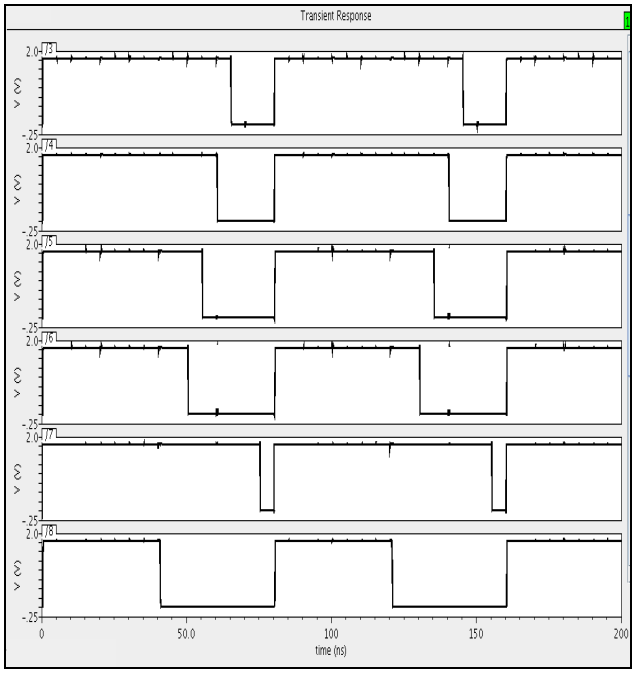

Figure 5 b) Simulation Result of Binary to Thermometer Decoder

7.DESIGN SPECIFICATION OF BINARY TO THERMOMETER DECODER

The Specifications utilized in designing the architecture of binary to thermometer decoder is shown in Table 1 which includes the technology used for architecture design, power consumption and time period upon which the output waveform is obtained.

Table 1

Technology	180nm
Resolution	4 bits
Supply Voltage	1.8 V
Period	80ns
Pulse Width	40ns

8.THERMOMETRIC DAC

For each value of digital input, the output changes as shown in output waveform of thermometer DAC in Fig. 6.

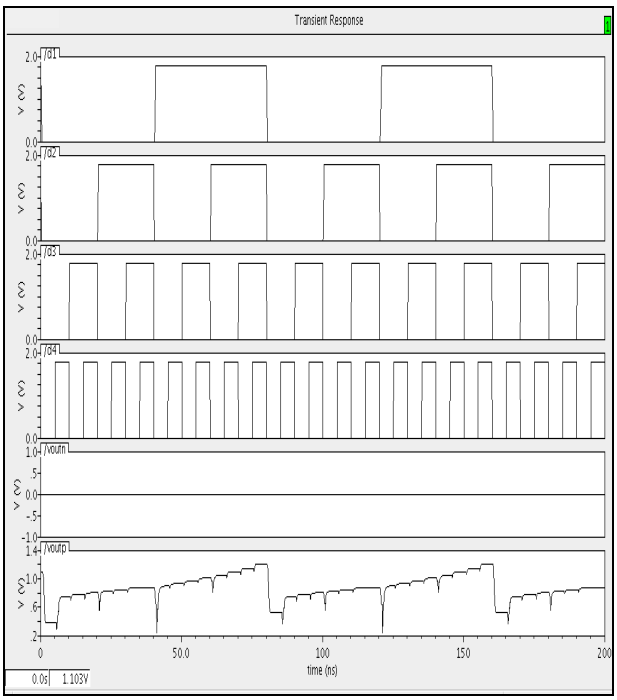

Figure 6 Simulation Result of Thermometer DAC

9. DESIGN SPECIFICATIONS OF THERMOMETER DAC

TABLE 2

Technology	180nm
Resolution	4 bits
Supply Voltage	1.8 V
Maximum Period	80ns
Stop Time	200ns
Full Scale Output Voltage	1.4 V
Power Consumption	2.4 mW

References

[1] Irfansyah, A.N, Lehmann, T., Jenkins, J., Hamilton, T.J., "Analysis and design considerations of systematic nonlinearity for sigma-delta current-steering DAC," IEEE Conference TENCON Spring,2013 , vol.no.111, pp.17-19 April 2013.

[2] Yonghua Cong, "Formulation of INL and DNL yield estimation in current-steering D/A converters," Circuits and Systems, 2002. ISCAS 2002. IEEE International Symposium on , vol.3, no., pp.III-149,III-152 vol.3, 2002 doi: 10.1109/ISCAS.2002.1010182

[3] Xueqing Li, Qi Wei, "Code-independent output impedance: A new approach to increasing the linearity of current-steering DACs," 18th IEEE International Conference on Electronics, Circuits and Systems (ICECS) 2011,, vol., no.11, pp.216,219, Dec.2011 doi:10.1109/ICECS 2011.6122252.

[4] Robert, J.; Temes, "A 16-bit low-voltage CMOS A/D converter," Solid-State Circuits, IEEE Journal of , vol.22, no.2, pp.157,163, Apr 1987 doi: 10.1109/JSSC.1987.1052697

[5] Sarkar, S.Banerjee, "An 8-bit 1.8 V 500 MSPS CMOS Segmented Current Steering DAC," IEEE Computer Society Annual Symposium on VLSI, 2009, vol.no., 13 pp.268,273, May2009.

[6] Myderrizi I., Zeki, "Current-Steering Digital-to-Analog Converters: Functional Specifications, Design Basics, and Behavioral Modeling," IEEE Antennas and Propagation Magazine , vol.52, no.4, pp.197,208, Aug. 2010.

[7] Yannan Ren, Fule Li, Chun Zhang, Zhihua Wang, "A 400MS/s 10-bit current-steering D/A converter," International Conference on Communications, Circuits and Systems, 2009. ICCCAS 2009 , vol., no.536, pp. 23-25 July 2009.