

# Design of 16 bit 180nm CMOS Fully Segmented DAC

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**Abstract:** Due to increasing advancement in technology in the field of digital signal processing, data converters such as analog to digital converters and digital to analog converters with high resolution are profoundly required but problem with incorporating these data converters induces non-linearity in the circuit mainly INL and DNL. Hence, In order to ameliorate the non-linearity, a review has been presented following various designs of segmented DAC which caters to implement the effective design of DAC with high resolution and monotonicity. The technique used to reduce the non-linearity has presented in detail. From this review, power consumption is highly reduced to large extent as well. This review paper would greatly assist the researchers and manufacturers to implement CMOS DAC with improved linearity which is essentially considered for numerous signal processing applications.

**Keywords:** CMOS DAC, INL, DNL, SFDR

## 1. INTRODUCTION

In recent decades, data converters are being highly utilized, the reason behind this is interfacing between digital data and analog world is required almost in every domain of signal processing such as telecommunication, wireless communication and image processing. Data converters such as digital to analog converter which constitutes signal processing are required to have good range of dynamic as well as static characteristics. For instance, spurious free dynamic range (SFDR) should be appropriate (in decibels) for efficient implementation of digital to analog converters. Moreover, there are many types of DAC's available which are designed and implemented based upon the specifications vital for the signal processing. Static performance is based on the anomalies like gain error, differential non-linearity (DNL), integral non-linearity (INL) and offset error while dynamic performance is affected by non-linearity such as glitches and time skew. Low power consumption and high speed performance became an important issue in data converters. In DAC, a single continuous output value in the shape of current or voltage is generated through a set of binary levels. The continuous type of signal in time and in amplitude is obtained from discrete type of signal in time and in amplitude with the reference input voltage applied to the data converters. Current steering DAC among various types of DAC's are popular because of the fact that these data converters provide higher resolution with less consumption of power. Current Steering Digital-to-Analog Converter has a fast speed of conversion and increasing resolution. Current Steering DAC is employed to enhance

the precision of matching of the Current sources. As it does not need an output buffer, so it is much better and faster as compared to other DACs such as Resistor Ladder and Resistor String. The basic technique of this DAC is to sum the currents from the current sources based on the digital input. The current sources are attached to output node with the help of MOS switches, which are managed by digital input code. Therefore, the current in the output node is relative to digital input code. Hence, for high speed and high resolution applications, Current Steering DAC is highly preferred [1]. The basic circuit of current steering data converter comprises of an array of current cells which includes matched current sources and switches as shown in Figure 1. The binary inputs control the switches. Current sources are bit dependent such that if the number of bits increases then the number of current sources increases. Switches drive the current from current sources to the output nodes. Operational amplifier is attached at the output such that the current is transformed into voltage[2].

## 2. SEGMENTATION

To utilize the benefits of two converters that is binary weighted and thermometer coded, both are combined together as represented in Figure 2. This architecture is designed in high resolution to provide a desirable performance.

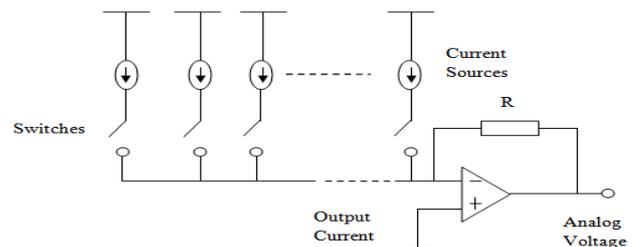


Figure 1 Current steering DAC

The combination of two architectures includes same type or different type of DAC. Since one DAC holds the most significant bit and another holds the least significant bit and outputs are finally accumulated. This technique is called Segmentation. For example: Consider a 7-bit Segmented DAC which is in such a way that 3-bit CMOS Thermometer-coded and 4-bit CMOS Binary weighted DAC is combined to achieve the advantages of both architectures. As described in the Figure 2, 3-bit

Thermometer-coded DAC comprises of seven current sources and switches such that a decoder is required which converts the binary code to thermometer code.

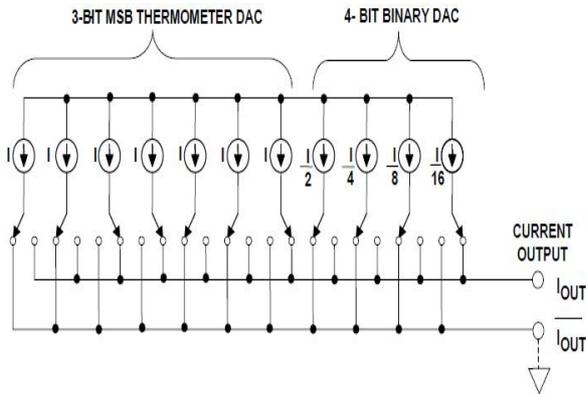


Figure 2 Segmented architecture of DAC

In case of binary-weighted architecture, N is number of bits.  $b_0$  to  $b_n$  are the binary inputs provided to the switches. Output Current is given by

$$I_{out} = b_0 I_{unit} + b_1 2^{-1} I_{unit} + \dots + b_N 2^{-N} I_{unit}$$

Thermometer-coded DAC employs current sources of equal value 'I'. 4-bit Binary DAC consists of four current sources and switches with each current source are of binary weighted value. Switches drive the total current to output nodes based on the digital input code. The percentage of segmentation is done in such a manner that optimized architecture is achieved. For instance, if there is 8-bit Segmented DAC with 4-bit CMOS Binary weighted and 4-bit CMOS thermometer-coded design then this architecture constitutes 50% Segmentation. And if this 8-bit Segmented DAC includes only 8-bit thermometer-coded DAC then it constitutes 100% Segmentation and this type of architecture is known as Fully Segmented digital to analog converter.

### 3. 8-BIT CMOS SEGMENTED DAC

Segmentation involves incorporating two different architectures of DAC into a single one to utilize the advantages of both architectures. Segmentation is generally acquired by the value of percentage such that if only thermometer coded DAC is designed and implemented using all the bits of resolution then at the point, it is required as 100% segmented architecture of DAC or fully segmented DAC. Likewise, 50% segmentation is achieved while utilizing equal amount of bits of both different architectures [4].

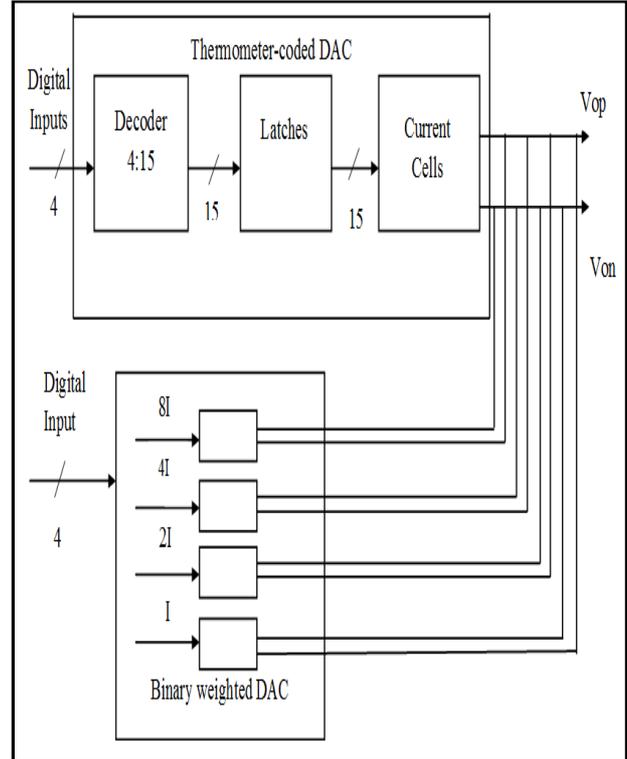


Figure 3 Block Diagram 8-bit Segmented DAC

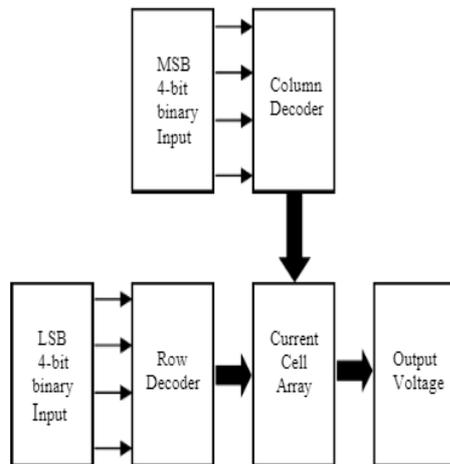
For instance, to design 8-bit segmented DAC, 4 bits of thermometer coded DAC are combined together and if implemented then architecture constitutes 50% Segmentation is achieved which has its own advantages as well as disadvantages.

The Figure 3 is representing the design of 8-bit segmented DAC with 50% segmentation with reduced complexity and non-linearity. Therefore, the variation in dynamic as well as static characteristics are being observed according to the percentage of segmentation in design such that the Integral Non-linearity (INL) and Differential Non-linearity (DNL) are reduced with higher percentage of segmentation. As presented in figure, for thermometer coded DAC, decoder is essential to decode the binary code to thermometer code. Code is illustrated in the Table 1. Latch is embedded in order to achieve synchronization, matching and to achieve accuracy. With 4-bits thermometer coded DAC, binary-weighted DAC architecture is incorporated to increase resolution. Binary-weighted DAC in figure 3 illustrating the current cells of current steering DAC are binary weighted which steers the equivalent amount of current to the output terminal;  $V_{op}$  and  $V_{on}$  that is one is positive terminal and other is negative and binary input is provided to the switches. 4-bit input is given to thermometer coded DAC and 4-bit input is given to binary-weighted DAC.

### 4. 8-BIT FULLY SEGMENTED DAC

The architecture of DAC which is designed and implemented with 100% segmentation is referred as Fully Segmented DAC. Fully Segmented architecture of DAC came into an existence because it incorporates many benefits of DAC such as reduced non-linearity. As illustrated in figure 4, 8-bits are been given to row and

column decoder such that 4-bits of MSB are utilized by column decoder and 4-bits of LSB are utilized by row decoder. Through Decoders, binary inputs are given to array current cells. From current cell, current is steered to the output with the help of switches. Current is transformed into voltage through op-amp[5].



**Figure 4** Block diagram of 8-bit Fully Segmented DAC

### 5. 16-BIT FULLY SEGMENTED DAC

Hence, 16-bit Segmented DAC can be designed and implemented utilizing two 8-bit fully segmented DAC such that one 8-bit DAC assist least significant bits and other 8-bit DAC assist most significant bits. In this way, the resolution is increased and linearity is improved with fully segmented DAC because fully segmented DAC is designed using thermometer coded DAC and advantage of thermometer coded DAC is that it has good linearity as compare to any other design of DAC. This Design can be implemented using Cadence Virtuoso Tool and utilized in various communication applications which require high resolution Digital to Analog converters.

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